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August 4, 1994

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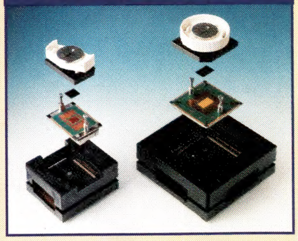

Temporary package yields low-cost known-good dice pg 13

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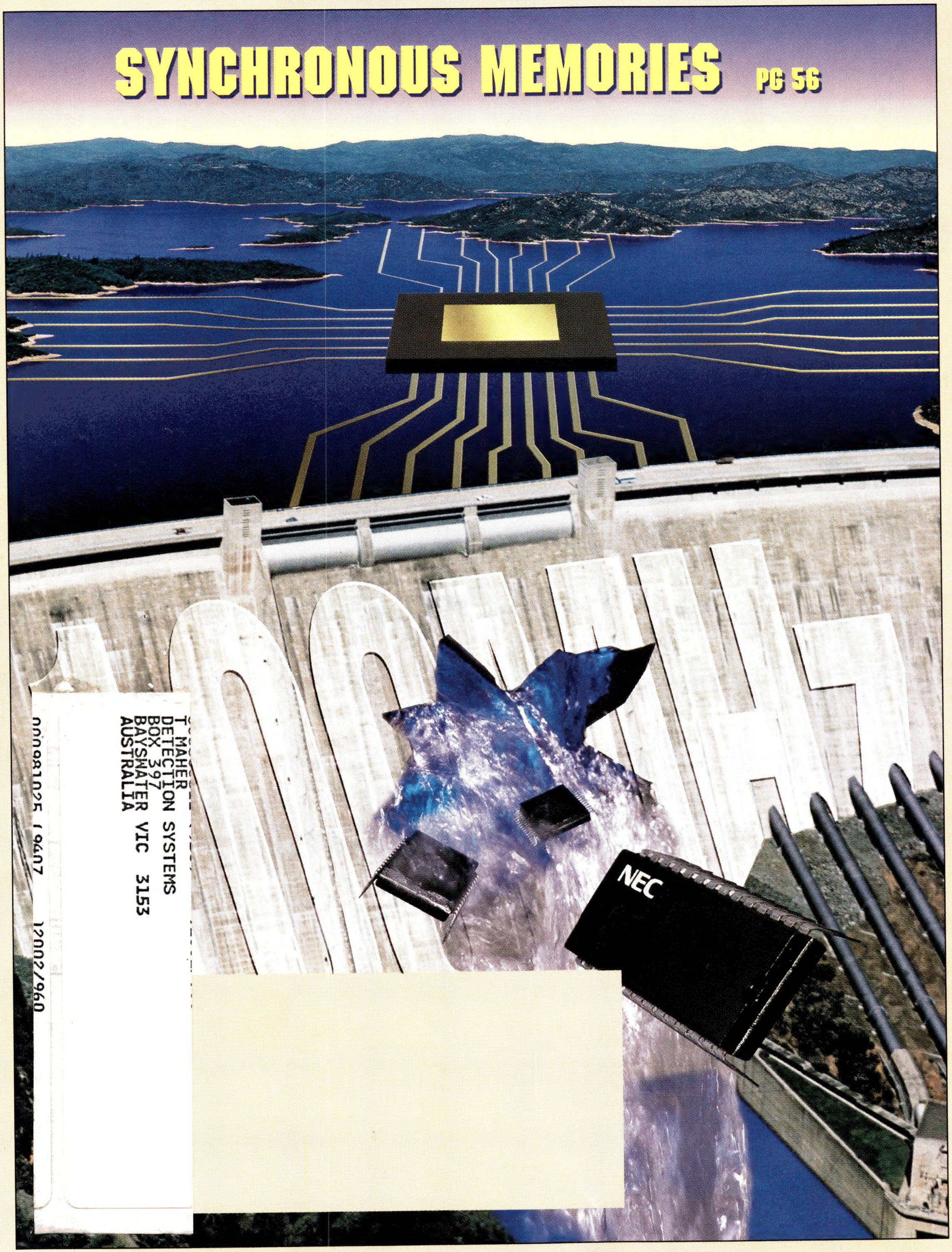

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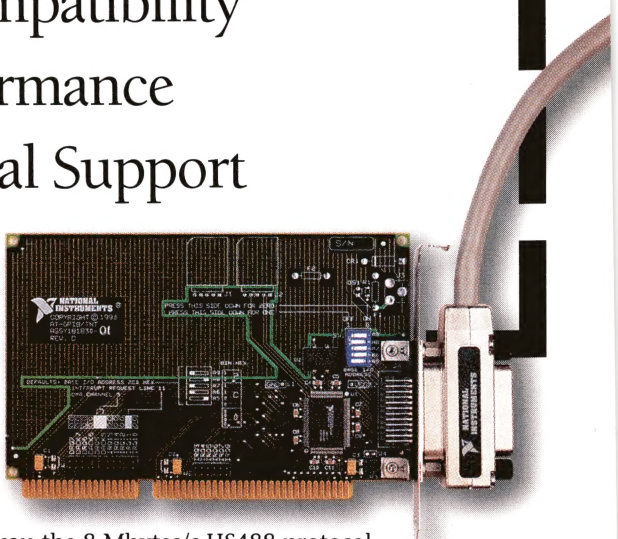
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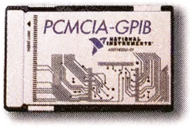

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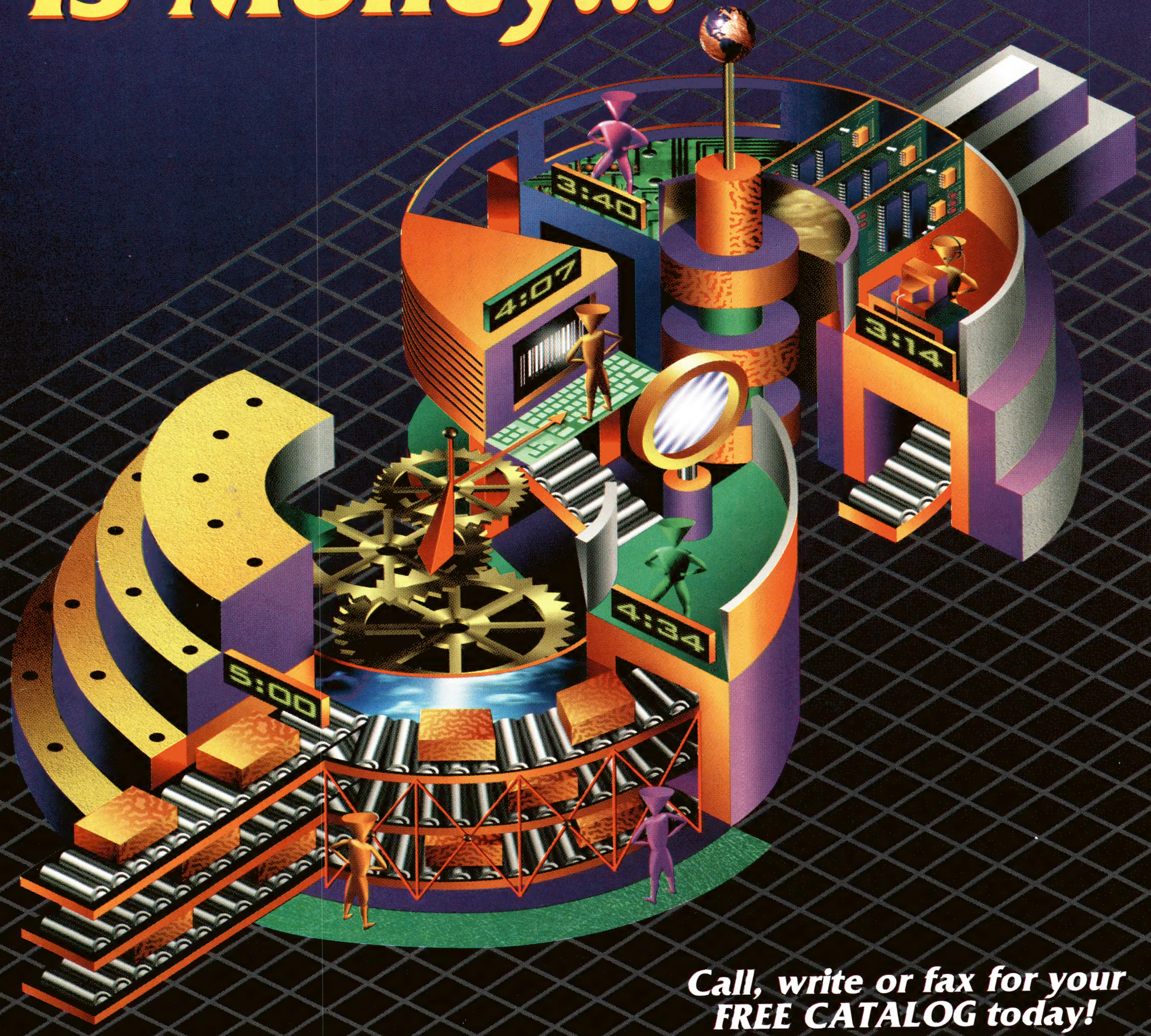

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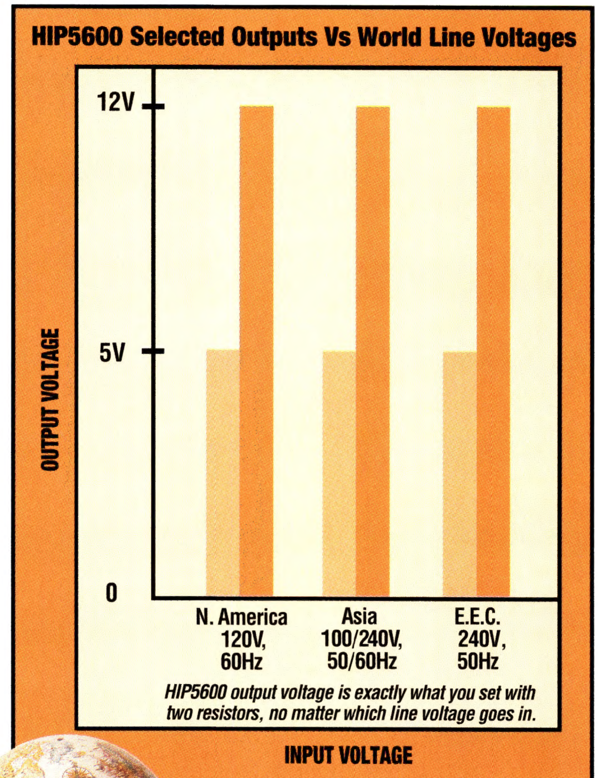

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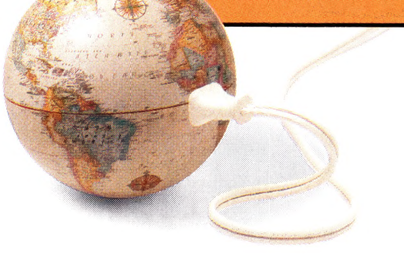

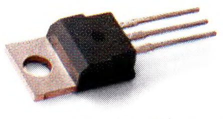

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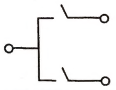

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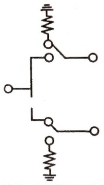

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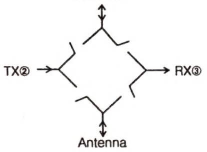

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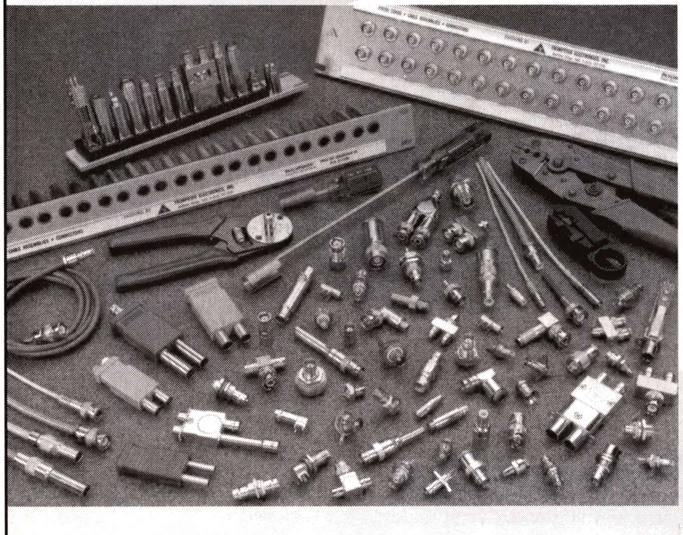

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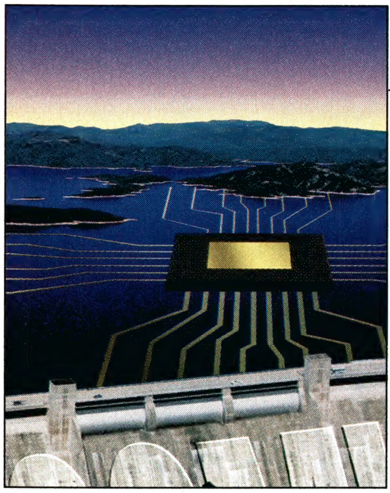

On the cover: Synchronous memories have burst on the scene to meet several demands: the increase in CPU clock speed and the integration of the primary cache memory into the processor die. See our Special Report, beginning on **pg 56**. (Photo courtesy NEC Electronics Inc)

SPECIAL REPORT

Synchronous memories 56

As system clock speeds push past 50 MHz, designers are discovering that asynchronous memory becomes unmanageable. As a result, they are looking to synchronous memories to handle increasing system speeds. What they are finding are new design challenges. *—Richard A Quinnell, Technical Editor*

DESIGN FEATURES

Noise-figure curves ease the selection of low-noise op amps 81

Evaluating plots of noise figure vs source resistance makes it easy to select a low-noise amplifier for a given source resistance. A BASIC program calculates the numbers from data-sheet parameters. *—John W Christensen, National Semiconductor Corp*

Canny choices condense CPLD and FPGA design cycles 91

The proliferation of CPLDs and FPGAs has resulted in flexible devices that reduce design time and contribute to a design's smaller size, higher reliability, lower cost, and lower power consumption. However, you must choose from among many devices, each having its own diverse architecture.*—Sung C Hu, San Francisco State University*

Embedded RISC µPs present new debugging challenges 105

Embedded systems based on RISC µPs offer many advantages but present unique debugging challenges. Although a logic analyzer isn't the only tool you need to meet these challenges, it is an important one, and you should consider making it the cornerstone of your debugging strategy.*—Roger Crooks, Tektronix Inc*

New philosophy aids shift from schematic-based to HDL-based design 119

Using HDL-based techniques for developing hardware is similar to using high-level languages to develop software: An object-oriented design philosophy is directly applicable.*—Charles F Shelor, Shelor Engineering*

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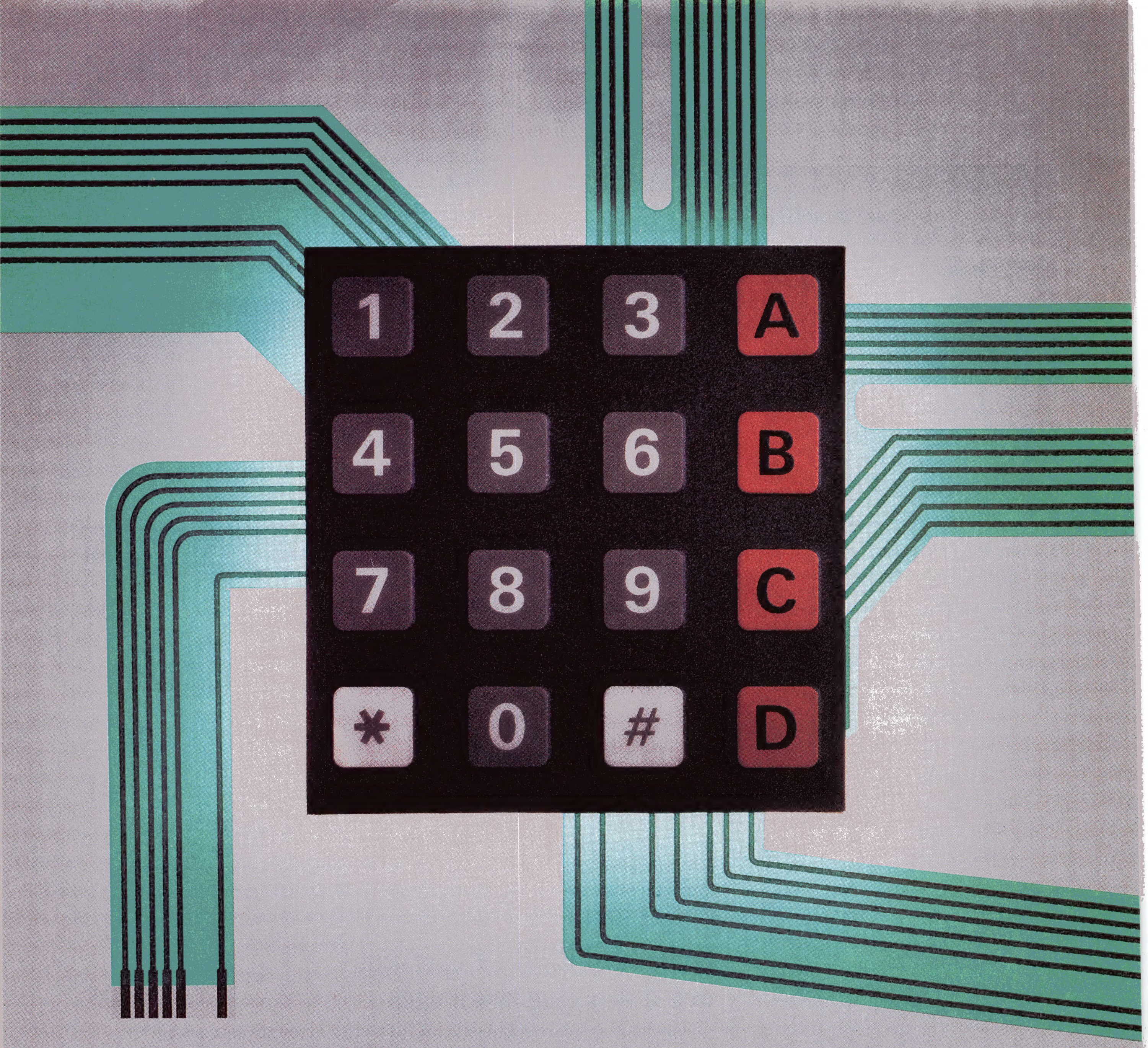

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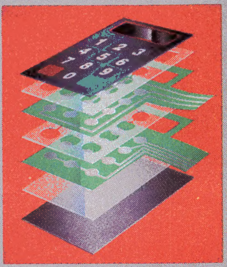

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TECHNOLOGY UPDATES

Software localization: Software vendors sweep aside language barriers 27

US software vendors face a dilemma: whether to thrust English-language products on foreign users or to "localize" products and offer their users native-language help, aide, ajuda, hjælp, hilfe, nápověda, ohje, pomoc, súgó, dowa juseyeo.—*Brian Kerridge, Senior Technical Editor*

Desktop DOS goes undercover to run embedded systems 43

Embedding a PC often involves embedding the most popular desktop operating system.—*David Shear, Technical Editor*

DESIGN IDEAS

RC network eliminates precision reference 71
Composite amplifier improves noise 71
Isolation transformer passes millihertz signals 72
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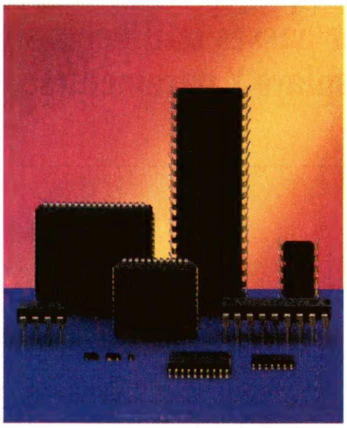

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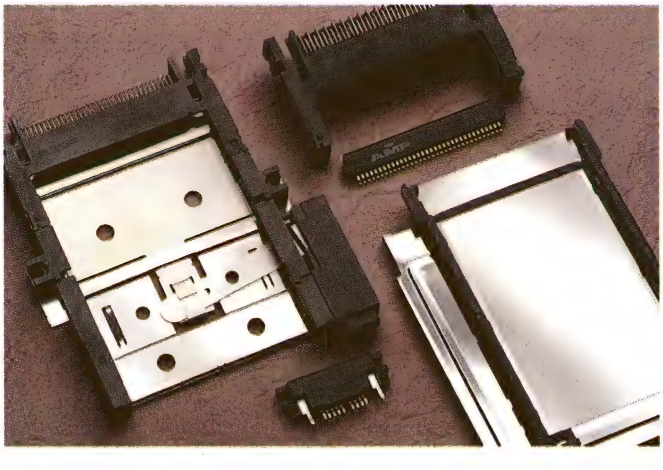

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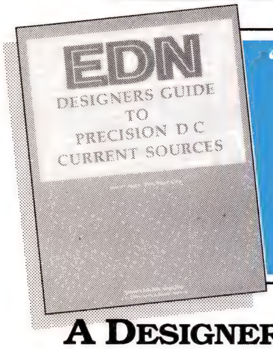
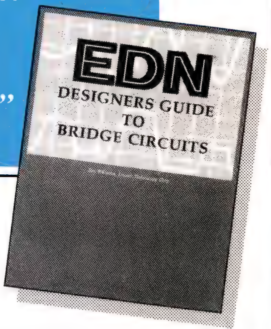


"You need only a resistor to convert a voltage to a current, but to convert accurately, the resistor voltage must ignore the load voltage."

◄ *A Designer's Guide to Precision DC Current Sources*

"A variety of tricks and techniques enhance the basic linearity, sensitivity, and stability of Wheatstone bridges."

A Designer's Guide to Bridge Circuits ►



A DESIGNER'S GUIDE TO PRECISION DC CURRENT SOURCES

BY JERALD GRAEME

This 3-part designer's guide shows you the fine art of designing, analyzing, and trimming accurate, stable dc current sources. This original, 18-page collection by Jerry Graeme—a prolific author on the subject of analog design—offers a wealth of information on how current sources work and how to analyze basic current-source circuits.

Jerry Graeme discusses and analyzes several circuits that use pairs of op amps. One of these circuits produces positive and negative current, which you can adjust through zero current. The Designer's Guide also shows you how to control current sources digitally. You'll find out that a current-output digital-to-analog converter may not be the best choice for a current source.

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BY JIM WILLIAMS

Bridge circuits are among the most elemental and powerful tools a designer has. They are used in measurement, switching, oscillator, and transducer applications. If you're interested in learning about bridge circuits from Jim Williams—a specialist in analog-circuit and instrumentation design—now's your chance. Order you own copy of EDN's Designer's Guide to Bridge Circuits. This guide will help you choose and design the circuit that's most appropriate for your application. In the first part of this guide, you'll learn about dc and pulsed methods for bridge-circuit signal conditioning. In the second part, Jim describes ac-driven bridges, which you'll find in specialized applications. Also included in this section are guides to distortion measurements and bridge interfaces.

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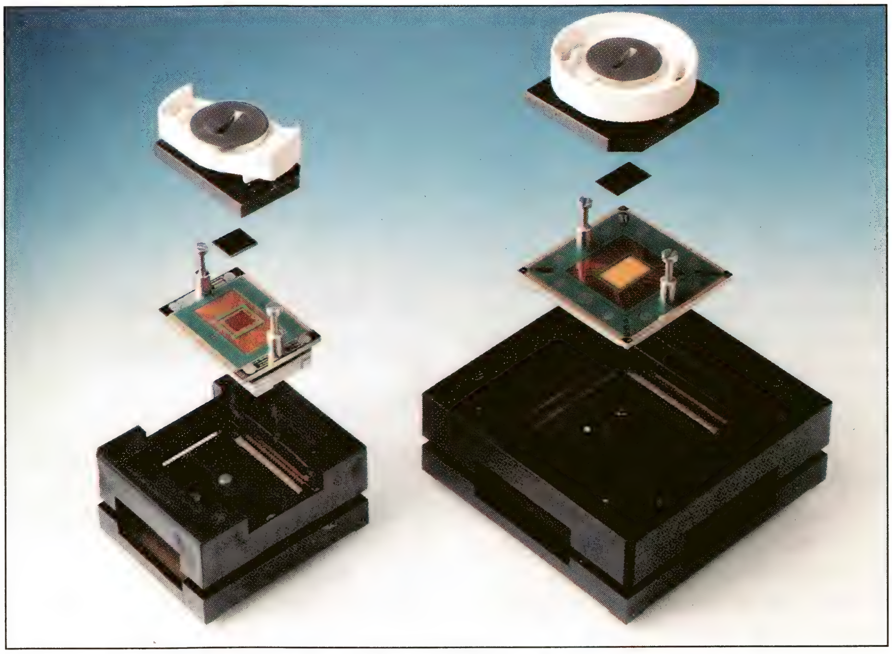
EDITED BY FRAN GRANVILLE

Temporary packaging yields reasonably priced KGD

Semiconductor manufacturers test virtually all of the packaged chips they ship and burn in many of them. One of the big problems facing designers of compact products—whether for military or commercial markets—is obtaining reasonably priced, uncased dice whose quality equals that of packaged chips. Such chips are called known-good dice (KGD). Techniques for testing fragile bare dice have been so costly and problematic that many manufacturers of assembled products (MCMs, for example) have resorted to using untested chips. This approach usually leads quickly from the frying pan into the fire: Only after expending high-priced labor do manufacturers discover which chips are defective. Assemblies that contain faulty chips must then undergo costly rework or make their way to the scrap heap.

For years, people throughout the industry have said they need a reliable, cost-effective method of testing and burning in uncased ICs. After years of development, Texas Instruments' Metallurgical Materials Div and MicroModule Systems (Cupertino, CA) has developed a temporary packaging system called DieMate. So far, one semiconductor vendor (Intel) has announced a line of uncased chips that are tested using the system. (Intel's trademark for the ICs is SmartDie.) Several other IC vendors are actively evaluating the DieMate technology.



A reusable temporary package, part of a system called DieMate, enables IC vendors to provide tested, burned-in uncased ICs to assemblers of MCMs and other compact products—at prices comparable to those of packaged chips.

A great deal of technology is involved. The heart of DieMate is a multilayer thin-film substrate unique to a particular chip layout. The substrate incorporates solder bumps that contact the chip's own bonding pads. (For bumped dice intended for face-down bonding, the substrate solder bumps contact the solder bumps on the chip.) The substrate also incorporates a dam that surrounds the chip's edges. The dam correctly positions the chip with respect to the substrate solder bumps. After the top is placed on the temporary package, the dam provides an environmental seal around the chip's edges, obviating the need for a clean-room environment.

Usually, pick-and-place machines will load the dice into the temporary packages. After that, the chips can travel to standard ATE using standard packaged-device handlers. For chip-level burn-in, the temporary packages plug into sockets mounted on cards that fit into standard burn-in racks. For high-volume burn-in, automated pick-and-place machines can install the temporary packages on the cards. After test and burn-in, pick-and-place machines unload the bare dice and place them in standard gel packs for shipment to assembled-product manufacturers. The temporary package is reused—up to 500 times.

TI estimates the cost of the system at between 25 and 50 cents per chip in high volume. The cost depends on the chip's size and complexity as well as its manufacturing volume. Especially for more complex chips, such costs compare favorably with those of conventional packages. Moreover, TI estimates that in MCMs, the savings from eliminating rework can range from 25 to 75% of an assembly's cost. Currently, TI makes the temporary packages in 56-, 110-, and 280-pin sizes. A 400-pin version is on the drawing board. The packages have been fully characterized for their high-speed properties at frequencies to 250 MHz.

—by Dan Strassberg

Texas Instruments Inc, Attleboro, MA, (508) 699-3800. **Circle No. 423**

PCMCIA disk drive stores 340 Mbytes

MiniStor Peripherals Corp is now shipping samples of a 1.8-in. disk drive that stores 340 Mbytes of compressed data. The Type III (10.5-mm-thick) PCMCIA card that contains the drive implements a data-compression algorithm from Stac Electronics in hardware, effectively doubling the drive's 171-Mbyte native capacity. Users may optionally disable compression.

The 340 MB More Drive, as the new product is called, joins a line of other PCMCIA disk drives noted for their ruggedness. The new drive, according to MiniStor, will withstand a 200-g shock while operating and a 900-g nonoperating shock. It has a suggested retail price of $599.

—by Gary Legg

MiniStor Peripherals Corp, San Jose, CA, (800) 943-0165. **Circle No. 424**

12-bit ADC's low distortion enables "soft" wireless basestations

By exhibiting a spurious-free dynamic range of 72 dBc at 13 MHz, Analog Devices' AD9026 and 9027 are suitable for wideband applications that require 70 dB of distortion-free dynamic range. One such example is the "soft" basestation for cellular communications. A conventional basestation requires up to 60 transceivers, one per cellular channel. The soft approach uses a single shared receiver to digitize the entire 12.5-MHz cellular bandwidth and then individually selects and processes each channel digitally. This technique is only commercially feasible using an ADC with a sampling rate of at least 31M samples/sec, wide dynamic range, and very low distortion.

The 9026 and 9027 have a 200-MHz analog-input bandwidth so they can down-convert band-limited signals with carrier frequencies in the 15- to 30-MHz range. The TTL 9026 and ECL 9027 are identical designs, apart from their output interface. Both integrate a reference, T/H amplifier, output logic, and internal bypass capacitors. Power consumption is 1.6W with 5 and –5.2V supplies. S/N ratio plus distortion is 63 dB for full-scale inputs at 13.4 MHz. Intermodulation distortion is better than 76 dB for two tones at 9.6 and 11.3 MHz, each 7 dB below full scale. The devices cost $238 (1000).

—by Anne Watson Swager

Analog Devices, Wilmington, MA, (617) 937-1428. **Circle No. 425**

SCSI controller card achieves PCI compliance

The TMC-3260 SCSI-2 controller card from Future Domain is the first such card to achieve full compliance with the Peripheral Component Interface (PCI) 2.0 specification. The card, which plugs into a PCI slot, is autoconfiguring, requiring neither jumpers nor software settings. It is based on Future Domain's 36C70 PCI-to-SCSI IC.

PCI 2.0 compliance has both hardware and software requirements. At the hardware level, a card must support shared interrupts and interrupt chaining. At the software level, it must work with a variety of operating systems. It must also contain a descriptive PCI "header" and provide automatic, active termination. The TMC-3260 card, for example, senses if it is in the middle of the SCSI bus and disables termination. The card sells for $139 by itself or, with cable and software, $195. —by Gary Legg

Future Domain Corp, Irvine, CA, (714) 253-0400. **Circle No. 426**

Air Force policy and procedures available electronically

The US Air Force Publications Distribution Library has selected InfoAccess Inc's Guide to Professional Publishers to deliver electronic versions of Air Force documents to more than 600,000 users at 2600 squadron-level units. The system will convert various media sources into one electronic text and graphics database, providing access to interactive versions of all publications, such as policies and procedures. The system links related passages in the information database and performs searches for key words and phrases.

—by Fran Granville

InfoAccess Inc, Bellevue, WA, (206) 747-3203. **Circle No. 427**

US engineers experience more age discrimination

US electrical, electronics, and computer engineers in their 50s and 60s report higher rates of unemployment, self-employment, and forced retirement than their counterparts in other countries, according to an IEEE US Activities (IEEE-USA) survey. The random survey polled 970 US IEEE members and 1130 non-US members. The US engineers also reported greater pressure to retire than their foreign counterparts: 32% of US engineers say they retired involuntarily, compared with 26% of non-US retirees. The survey also revealed that the average salary of US engineers is $59,754, and typical salaries range from $70,000 to $90,000. You can get a copy of the survey from IEEE-USA.—by Fran Granville

IEEE-USA, Washington, DC, (202) 785-0017. **Circle No. 428**

16-bit I/O card needs no jumpers

The 16-bit Soft I/O card for IBM and compatible machines requires no jumpers and provides four high-speed serial ports and two bidirectional printer ports. Using the device and software, users can change the address or disable any of the serial and parallel ports as well as select from interrupts 3, 4, 5, 7, 9, 10, 11, 12, and 15 for any port. The hardware is register-level-compatible with high-speed 16550-type UARTs with internal 16-byte buffers and IBM PS/2 printer ports. The device also supports onboard BIOS support for future expansion through a flash BIOS. Applications for the serial ports include 9600-baud external modems, and the bidirectional ports permit using scanners and faster data transfer for laser printers and external printer-port-driven tape drives. Price for the Soft I/O is $299 (Canadian).—by Fran Granville

Axxon Computer Corp, Windsor, ON, Canada, (519) 974-0163.

Circle No. 429

SHORTS

I-Cube signs distribution agreement. I-Cube Inc, a manufacturer of field-programmable interconnect devices, has signed a distribution agreement with Insight Electronics, San Diego. Under terms of the agreement, Insight will distribute I-Cube products throughout North America and serve as a manufacturer's sales representative in territories where I-Cube has no other contracted representatives. I-Cube Inc, Santa Clara, CA, (408) 986-1077. **Circle No. 430**

EEPA changes name. The Electromagnetic Energy Policy Alliance has changed its name to the Electromagnetic Energy Association. It has also expanded its purpose to establish ANSI-accredited product and industry standards for EMF use and to provide public education for EMF safety. EEA, Washington, DC, (202) 452-1070.' **Circle No. 431**

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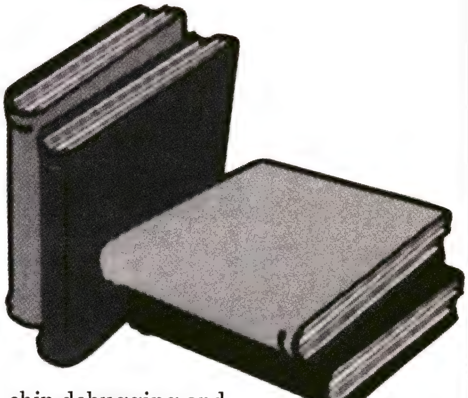
DSP book replaces expensive consulting services



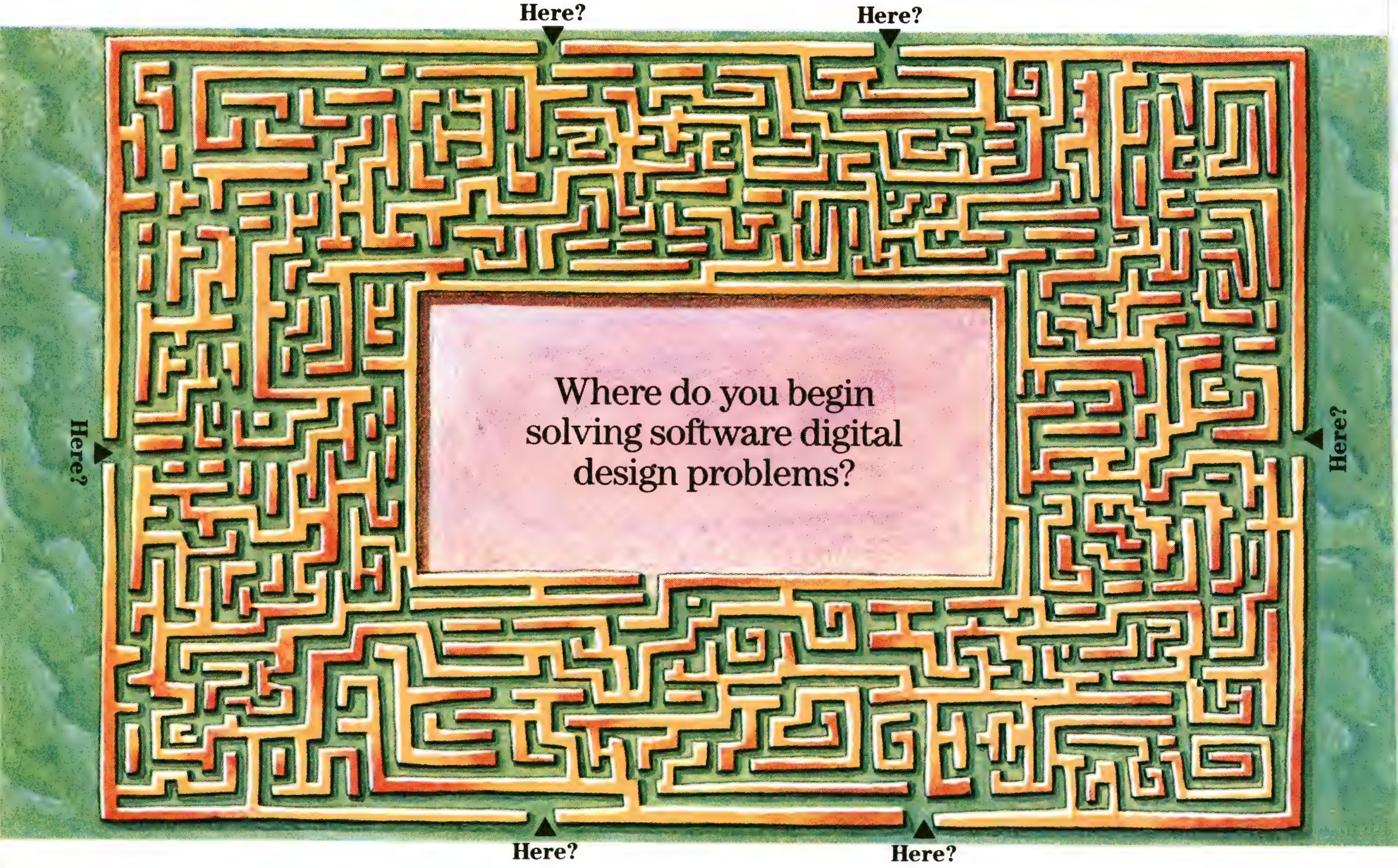
The price of *A Buyer's Guide to DSP Processors*, by Berkeley Design Technology Inc (Fremont, CA) alone should intrigue you. At $1850 for the first copy and $400 for additional copies, this is more than just a book; it is a 666-pg report that provides a comprehensive marketing and technical guide to programmable DSPs (digital signal processors). The book states: "This report is intended for anyone who is evaluating or comparing DSP processors, or who wants an independent, comprehensive introduction to the technology."

After the basic introductory chapters, the book really begins in Chapter 3 with a quick look at the fundamentals of DSP: What is DSP? What are DSP processors and their applications? DSPs are popping up everywhere and this chapter explains where they fit in.

Chapter 4, entitled "Embodiments and Alternatives" briefly describes the various formats that DSP hardware can assume: from multichip modules, to DSP cores, to multiprocessors. The chapter also discusses some of the alternatives to using commercial DSP processors.

The next chapter, "Characteristics of DSP Processors," is where the real action begins. For someone coming up to speed on this subject, this chapter is great. Although you won't walk away an expert on DSP (this would require years of schooling), you'll learn enough to talk intelligently about it. Topics in the chapter include the difference between floating- and fixed-point processing, DSP data paths and memory architectures, addressing modes and instruction sets, execution control (eg, looping and interrupts), pipelining, peripherals, power consumption and management, and on-chip debugging and development tools. The best part about this chapter is that the material provides a lot of useful and interesting details in an easily comprehensible form. Furthermore, it doesn't bog you down with the overwhelming amounts of mathematical equations normally packed into textbooks.

Chapter 6 describes how to choose a processor that will satisfy the requirements of your projects. I especially appreciated the way that the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Where do you begin solving software digital design problems?
Here?
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book presented this using common DSP-related examples such as modems, disk-drive servo-control, and PC multimedia. This allows you to get a good feel for how DSP fits in from a practical perspective. You'll also find the discussion on application profiling (a technique for measuring/estimating the time a program spends in its various subsections) useful because this is probably how you'll determine the performance the DSP requires.

Chapters 7 and 8 deliver an unbiased description of the features of 23 industry-leading DSPs in detail. If you're already an expert on DSP, this is where you'll get your money's worth out of this book. You can comb through hundreds of pages of organized and carefully analyzed information. Each processor is examined for its architecture, instruction set, execution control, peripherals, on-chip debugging support, development tools, power consumption, advantages, and, most importantly, its disadvantages. From these descriptions you'll definitely be able to choose the DSP for your application, and it sure beats having to painstakingly sort through piles of data sheets. On the other hand, if you're trying to design a processor, you'll find these chapters useful for understanding what the competition is doing.

The last chapter tackles benchmarking—the "smoke and mirrors" of the DSP vendor's marketing tactics. For example, how valuable is benchmarking in terms of MIPS (millions of instructions per second), when one processor takes 100 instructions to perform an operation and another processor can perform the same operation in two instructions? In this chapter, the BDT team presents the benchmark procedures and data they developed and organized for the DSPs discussed in this book.

Overall, I found this book to be very readable and well organized. Furthermore, it provides a great replacement for a seminar (which would probably cost more than the book and wouldn't contain nearly as much information). Unlike many technical books that are outdated the instant they're printed, you can receive updated information by mailing in your book's registration card. Combine *A Buyer's Guide to DSP Processors* with *EDN's DSP-Chip Directory* (*EDN*, June 9, 1994, pg 75), and you'll have just about everything you need to understand what's happening in the DSP market.

—Markus Levy

Forward Concepts, Tempe, AZ. (602) 968-3759. **Circle No. 500**

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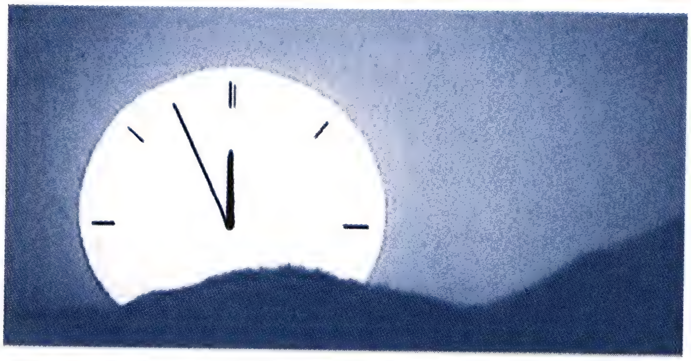

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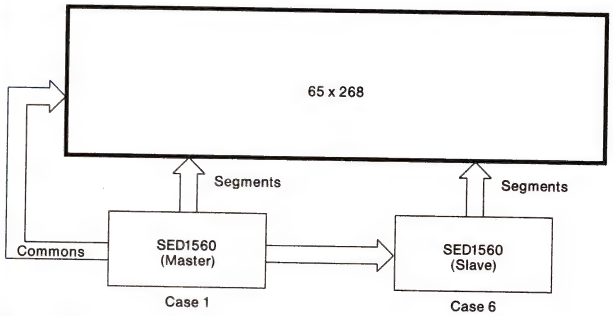

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Power-components catalog. A 36-pg color catalog describes the company's full line of component and configurable power products. The guide includes photographs, descriptions, technical specifications, applications information, and selection charts. **Vicor Corp**, Andover, MA. **Circle No. 415**

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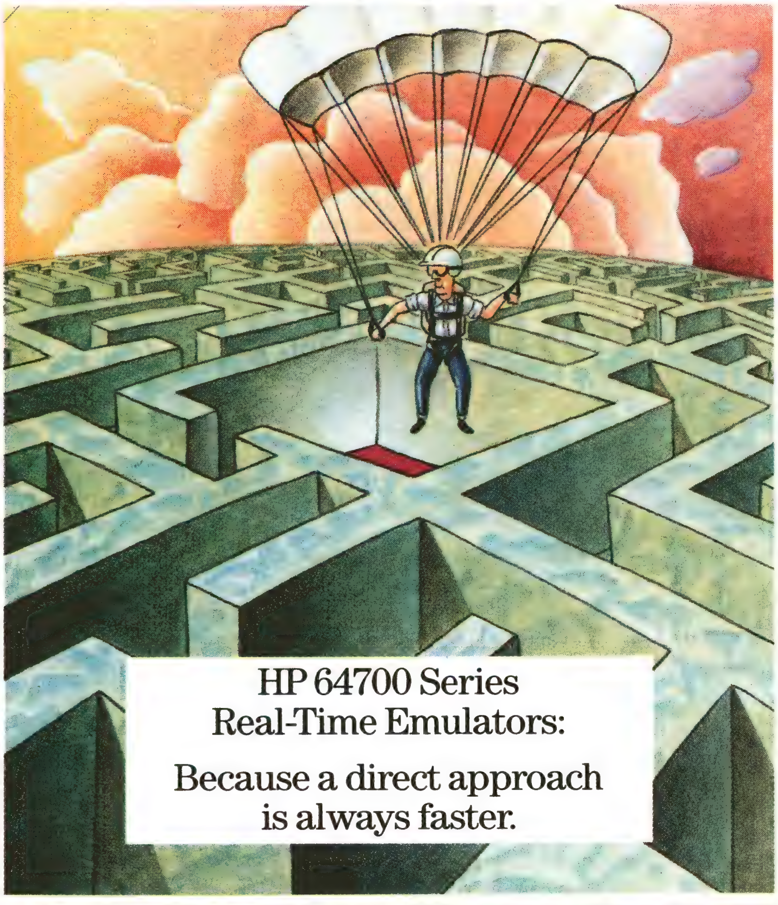
Shortform catalog on test and digital-multimeter accessories. This shortform catalog provides information on test connectors and digital multimeter accessories for electronic R&D labs, workstations, service departments, electricians, and training institutions. The guide also describes a line of test probes, clips, and leads for electrical and electronic test-and-measurement applications. **Hirschmann of America Inc**, Riverdale, NJ. **Circle No. 416**

Catalog features high-power resistors and terminations. This 6-pg brochure details a line of high-power resistors and terminations. The catalog describes models with power handling from 10 to 800W, with values ranging from 0.5 to 20,000Ω. Designed for use in high-power amplifiers, the resistors and terminations are ideal in microstrip applications. **RF Power Components Inc**, Holbrook, NY. **Circle No. 417**

Software catalog and free demo disk. A free catalog with demo disk describes a multitasking, object-oriented software package designed to simplify creating custom test, measurement, and data-acquisition applications in the Microsoft Windows environment without the need for conventional programming techniques. **Keithley Instruments Inc**, Cleveland, OH. **Circle No. 418**

Application note explain amplifier intermodulation test station. This 20-pg brochure details a new UFX-NPR amplifier test station, designed to measure intermodulation distortion and spectral regrowth using the noise-power-ratio (NPR) method. **Noise Com Inc**, Paramus, NJ. **Circle No. 419**

Infocard on Pentium power products. A free 4-pg infocard provides information on linear and switching voltage regulators for use with Intel's Pentium microprocessor. It covers five regulators that deliver 3.3V efficiently from a 5V supply at currents ranging from 1.5 to 10A. The infocard also includes a table of RS-232C serial-port ICs that are compatible with 3V logic. **Linear Technology Corp**, Milpitas, CA. **Circle No. 420**



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Steven H. Leibson

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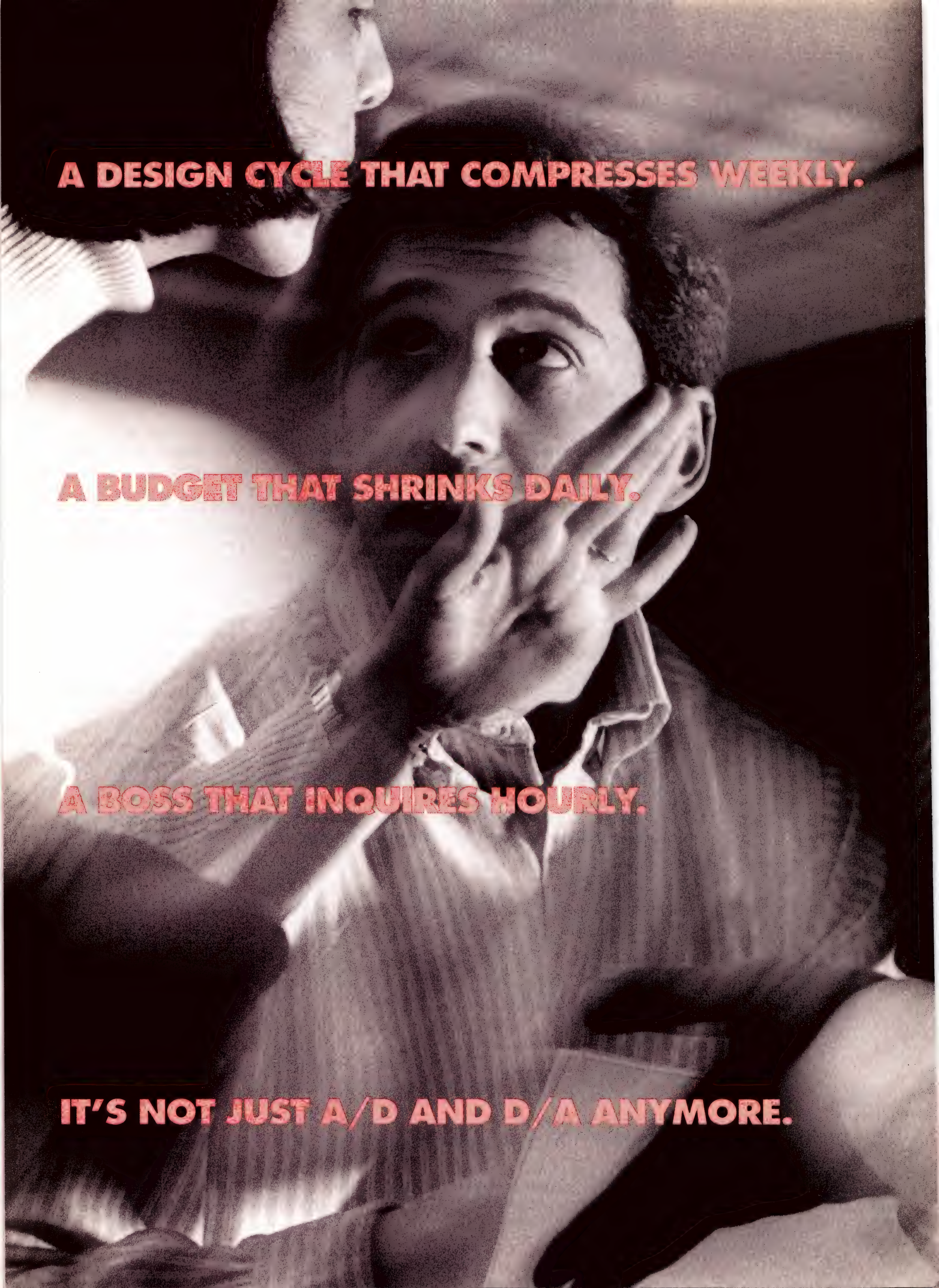
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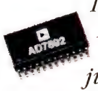

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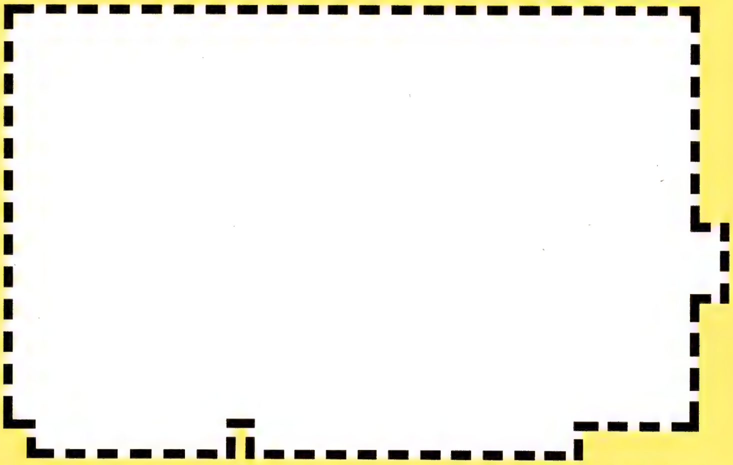

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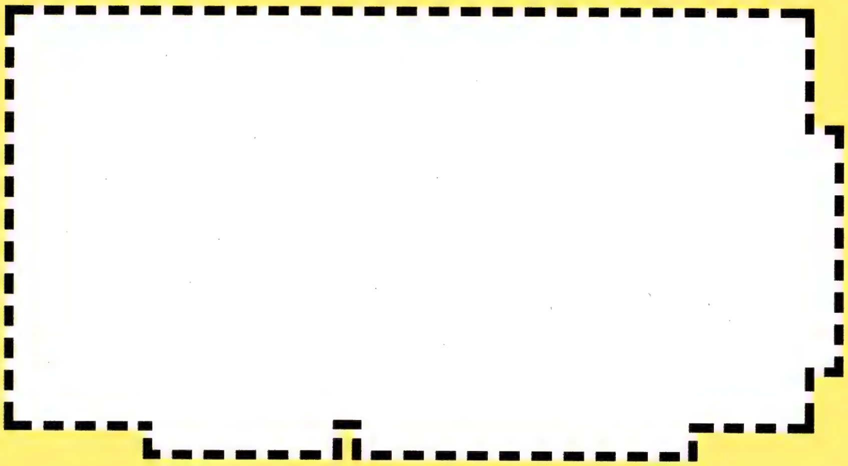

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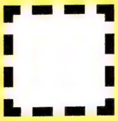

AMD's PCnet-SCSI controller: 1 1/8 x 1 1/8 inches.

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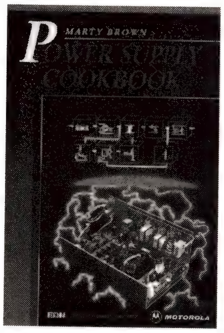

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SOFTWARE LOCALIZATION

Software vendors sweep aside language barriers

BRIAN KERRIDGE, Senior Technical Editor

US software vendors face a dilemma: whether to thrust English-language products on foreign users or to "localize" products and offer their users native-language help, aide, ajuda, hjælp, hilfe, nápověda, ohje, pomoc, súgó, dowa juseyeo...

The next time you power up a PC, imagine viewing a file menu in French, a dialog box in Czech, or a date in Chinese. Not what you'd call "user-friendly," but, nonetheless, examples of what many foreign users face daily with English-language software applications.

One way to offer foreign users the same level of convenience, comprehension, and satisfaction that native English speakers enjoy is "software localization"—a facility that makes software communicate with users in their native language.

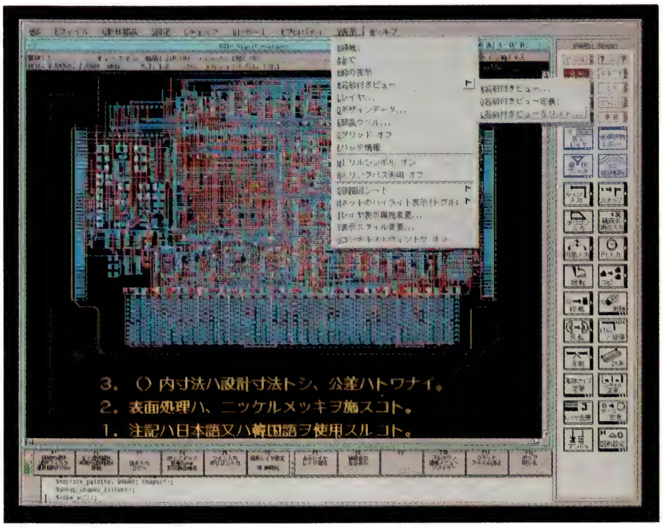
Although they accept localization as a desirable and laudable objective, developers of scientific and engineering application software have been slow to offer localized products. Much of the reason stems from a belief that localization means facing intractable language problems. Supporting applications in one language is generally enough of a problem, they believe, without having to add as many as 30 other versions.

In fact, some developers avoid the issue altogether and voice a popular argument that their foreign users are mainly scientists and engineers, who are already English literates. Other reasons vendors express for not localizing their products relate to cost, loss of quality control, and extended time to market.

Despite these arguments, communicating with a PC is, by definition, personal, a tête à tête involving a user and a powerful tool. Anything less than 100% communication implies proportionately less efficient use of the tool's functions.

It's true that a well-designed graphical user interface (GUI) can minimize the requirement for textual communication and works fine for day-to-day operation, once a user is familiar with a product. But when running a tutorial or when operation takes an unexpected turn, the user needs to understand text messages or to head for a help menu.

No doubt many global users accept English software applications. But, in most cases, it's because they have no alternative, and locally developed alternatives, when available, offer limited capability and support. Even English-speaking foreign scientists and engineers, given the choice, prefer communicating in their native languages. Additionally, where applications communi-



3. （）内寸法ハ設計寸法トシ、公差ハトワナイ。
2. 表面処理ハ、ニッケルメッキヲ施スコト。
1. 注記ハ日本語又ハ韓国語ヲ使用スルコト。

Mentor Graphics has structured its EDA products so that localization requires no access to source code. Company policy encourages national offices to localize products based on market requirements. Currently, Mentor's Japanese and Swedish offices offer localized versions.

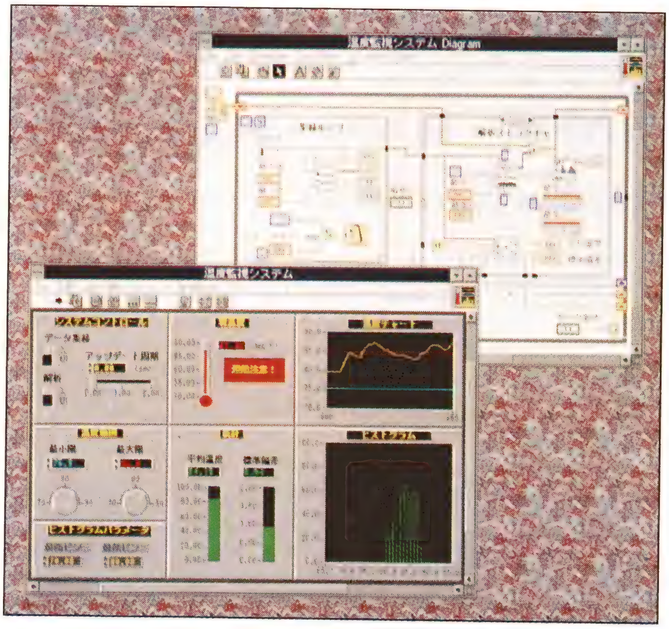
cate with technicians and unskilled operators, English-language software may be unusable.

If you want to localize software products, the obstacles are formidable but not insurmountable. Much depends on the level of localization you are targeting. At a basic level, simply translating screen text is straightforward. Adding processing of user inputs for one localized language is more complex, and expanding that facility across multiple languages significantly increases the challenge.

Ideally, you need to lay foundations for localization at the outset of development. For example, you need to partition screen text from operational code for your application. Also, you need to consider which markets to target for localization. Japan comes high on the list of priorities, and that means your application must support a double-byte character set; US and most European-language software uses single-byte characters.

Fortunately, companies such as Microsoft and Apple have pioneered this territory in their advances on domestic and home users. As a result, MS-Windows and Macintosh developers find many of the architectural features and facilities for localization built into the development tools.

In addition, there are plenty of subcontract companies specializing in software localization. Generally, these companies offer wider localization services, including translating support documentation, developing glossaries, and distributing software.



National Instruments localized Japanese LabView software displays dialog-box and menu-bar information using double-byte kanji characters.

These localizers accept MS-DOS, MS-Windows, Macintosh, and Unix applications.

RR Donnelley Information Services is a major company in the information-translation business. Software localization accounts for around 40% of the company's revenue, and 80% of that work involves translating MS-Windows applications. The company operates from 10 offices around Europe and one in Beijing. The company localizes products into 15 European languages—principally French, German, Italian, and Spanish—and into Chinese, Japanese, and Korean.

David Roach, vice president and director of business development at Donnelley, explains that the company's service extends beyond straightforward translation to include creating, managing, and distributing information. Reducing customers' time to reach global markets is a primary focus of the company's service.

As an example, Roach cites work for companies such as IBM and Microsoft, where it once took up to nine additional months to release foreign-language software. Now, it takes three to four weeks maximum. Roach says these time-to-market reductions for localized products are broadly in line with speedier hardware developments: Five years ago, it took two to three years to develop a PC; now, it takes three to six months.

To attain this level of service, Roach describes Donnelley's hub-and-spoke strategy, which centralizes nonlanguage activities, such as preprocessing, setting up glossaries, and handling stylistic issues, and places these services on line in Donnelley's national offices.

UNICODE CHARACTER SET AIDS SOFTWARE LOCALIZATION

Most software applications support single-byte character sets, or code pages. As an example, European MS-DOS supports six single-byte sets, in which the first 128 characters of each set are common. The remaining characters in each set diverge to represent local- and national-language differences, such as accented characters and currency signs.

Problems arise when you need more than 256 characters to communicate, as with Asian languages. In this case, your software needs to support double-byte character sets.

In the late 1980s, a consortium of major software and computer companies, including Apple, Microsoft, and Sun Microsystems, set about developing one standard double-byte character set—known as "unicode"—to incorporate every conceivable international character likely to fall into use. Much of the work involved deciding how to reduce the large number of Asian-language characters to a workable selection. Known as "Han unification," the consortium reduced around 120,000 possible Chinese, Japanese, and Korean characters to approximately 20,000.

The work of the unicode consortium resulted in the international standard ISO 10646, "Basic Multilingual Plane."

Until recently, software support for unicode has been poor, but Windows-NT now offers support, so applications supporting unicode will follow.

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Roach stresses the importance of localizing products within the target country and of using staff with both development and end-user expertise. Without this arrangement, you can hope neither to incorporate cultural and straightforward translation issues nor to maintain the quality of a localized product. Roach believes that, because of the speed of changes in the information-technology sector, localizers should not spend more than six months away from their target countries. More than that will make them unattuned to the nuances of culture, colloquialisms, and jargon to maintain quality in localization.

Localization can be routine

Microsoft has more than a decade of experience in localizing its products and routinely offers software in as many as 30 languages. Although the company maintains a high level of in-house localization expertise, globally dispersed subcontractors perform most localization.

John Hopper, desktop-unit product manager at Microsoft, believes that localization involves more than just word translation. He says, in general, you also have to consider language structure and cultural issues. There are additional problems with languages that don't use a Roman alphabet and that require right-to-left page layout.

Some of the challenge is translating the jargon that US marketers create from bits of other words, which make sense only in English. One example is Microsoft's use of "wizard," which, when translated literally into other languages, may convey a meaning different from what Microsoft wants to imply.

Another basic problem is providing sufficient character fields for localized versions. For example, Microsoft's German translation of "undo" becomes "Rückgängig," and "preferences" becomes "Bildschirmeinstellungen," both too long to fit in the fields required for the US version.

Also, localization extends to packaging where color plays an important part. In some countries, purple has strong deathly connotations—clearly unsuitable for a "new-version" banner.

Hopper explains that word order poses further problems because software constructs expressions by pulling words from areas of code. A word order in English commonly doesn't track into a local language. For example, the word order in the string "Place disk 1 into drive A," which typically uses 4 bits of text, is incorrect in other languages.

Similar errors arise when using a fill-in algorithm with time and date information. In some countries, Monday, not Sunday, is the first day of week, and date format expects a year to be read first. In addition, some languages use a colon, a period, or a space as a character separator. Overcoming these problems requires small changes to the structure of the software as well as to the translation of text.

Hopper says an overall objective for those software developers anticipating localization should be to confine information for translation in a dynamic-link library (DLL). Then, when the software composes a string, it calls on the DLL, which returns the text. In an ideal situation, that arrangement means that localization needs access only to the DLL, minimizing the chance of interference with the software's fundamental operation. Hop-

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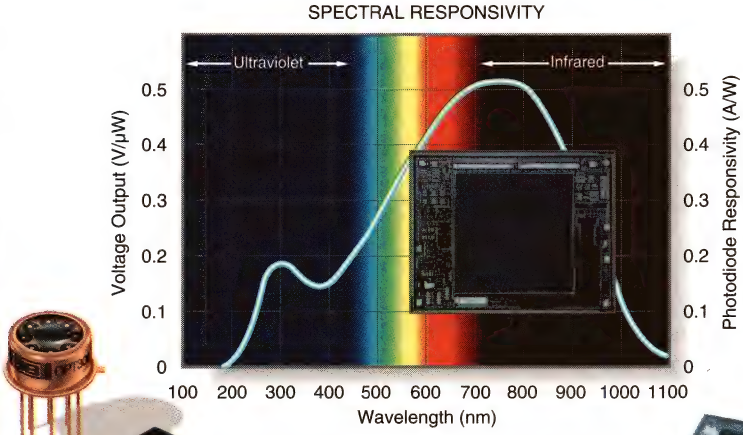

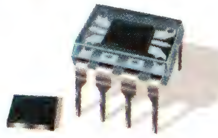

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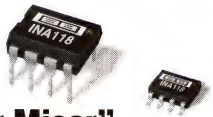

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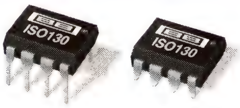

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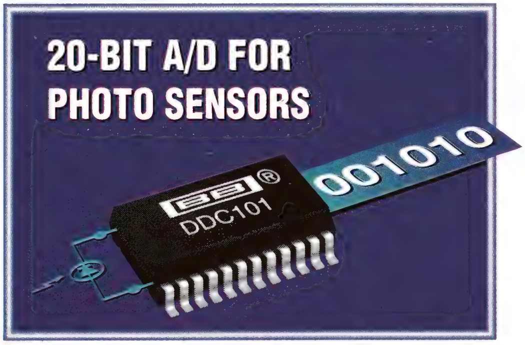
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per says one alternative is for localizers to edit tokens, or resource libraries. But that alternative means that they have to retest the product for basic functionality.

With a wealth of localizing experience, Microsoft developers anticipate many difficulties when designing a base product in English. Despite this experience, Microsoft often develops localized versions in parallel with the base product to highlight problems early. Following this strategy, the company routinely launches seven localized versions of products such as MS-Windows simultaneously with the US base version.

One problem Microsoft has identified is a need to maintain consistency in translation across a variety of products and revisions. For MS-Windows developers, Microsoft publishes a GUI guide (**Ref 1**) that offers localization guidelines for the main components of Windows and includes a glossary in 14 languages.

LOOKING AHEAD

Despite obvious marketing attractions, it's likely that engineering-software vendors will remain circumspect about localizing their products. Vendors report that Japanese users are the ones crying out for a localized version. Some vendors have already responded to that call, and others will feel compelled to follow.

As developers initiate designs and as support for unicode increases, companies will find it easier to lay foundations for future localizing opportunities.

Japanese is high priority

National Instruments offers a Japanese-localized version of its Macintosh LabView instrumentation-software system. The company has limited localization of LabView to translation of the dialog box and menu bars. This work involved introducing double-byte characters and localizing displayed text in kanji characters on LabView.

According to Paul Austin, software engineer with National Instruments, you need to decide at the outset of a design which level of software localization you want to reach. At a basic level, translation of dialog boxes and menu bars on a user interface is straightforward using readily available standalone tools.

A second level is to process localized data to provide data entry, to save program or configuration settings, or to operate a search facility. At this level, you need to employ system functions for Windows and the Macintosh. For example, system functions for sorting strings can depend on your locale. Using these functions

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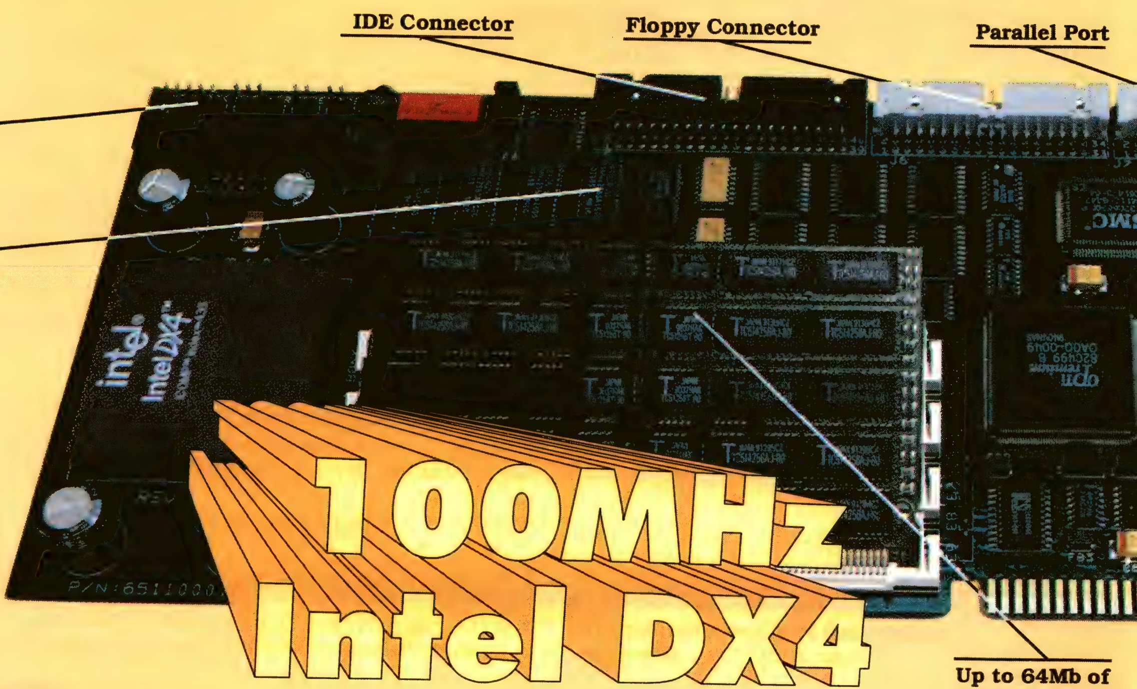
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makes much of the localizing effort transparent.

At the final level, Austin says, there's a difference in complexity between writing an application to be localized in just one language and one you expect to localize in several versions. Austin's general advice is to be not too ambitious in constructing long sentences. There are simply too many variations in sentence construction in different languages to expect to rebuild accurate lengthy text strings.

Racal-Redac Systems also offers a Japanese-localized product. The company has recently applied Japanese localization to the pc-board, multichip-module, and postprocessor tools in the company's Expert workstation electronic-design-automation suite. Duncan Hooper, senior development manager for CAD/CAM tools, says the company limited localization to warning and error messages and to input and output of design text. He says that, although system users can handle an English GUI, they must be able to read warning and error messages that signify unusual events. In addition, shop-floor operators have to be able to read manufacturing documents that the tools generate.

To generate documents in the Expert system, you have to type Japanese text, and the system must be able to plot out that information. Building in the facility to plot out Japanese characters proved to be a significant task. The characters require a vector font that can be stroke-drawn with a photographic or pen-plotting device, rather than simply referenced to a standard bit-map font, as with normal text output.

Hooper says a "locale" facility in Unix utility X11.R5 was instrumental in enabling Racal to produce a localized version. This facility aids the assembly of message catalogs of translatable text and handles multibyte characters for Japanese. The company assembled the message catalogs in its UK plant and carried out the translation at its Japanese office. EDN

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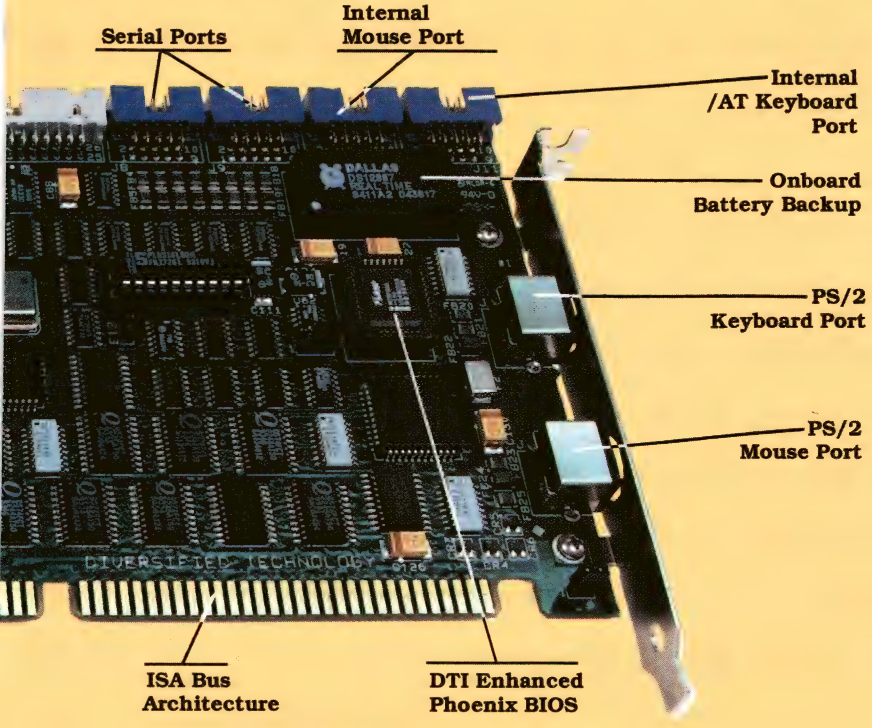

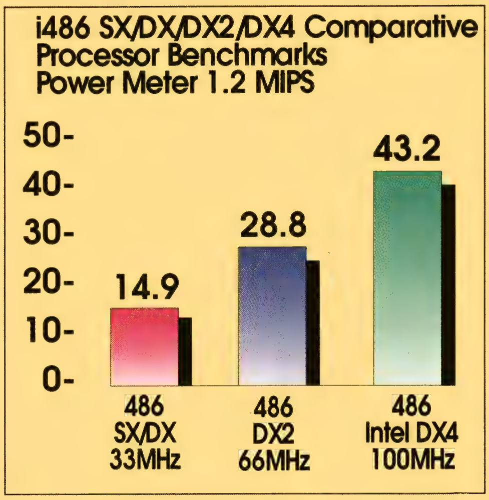

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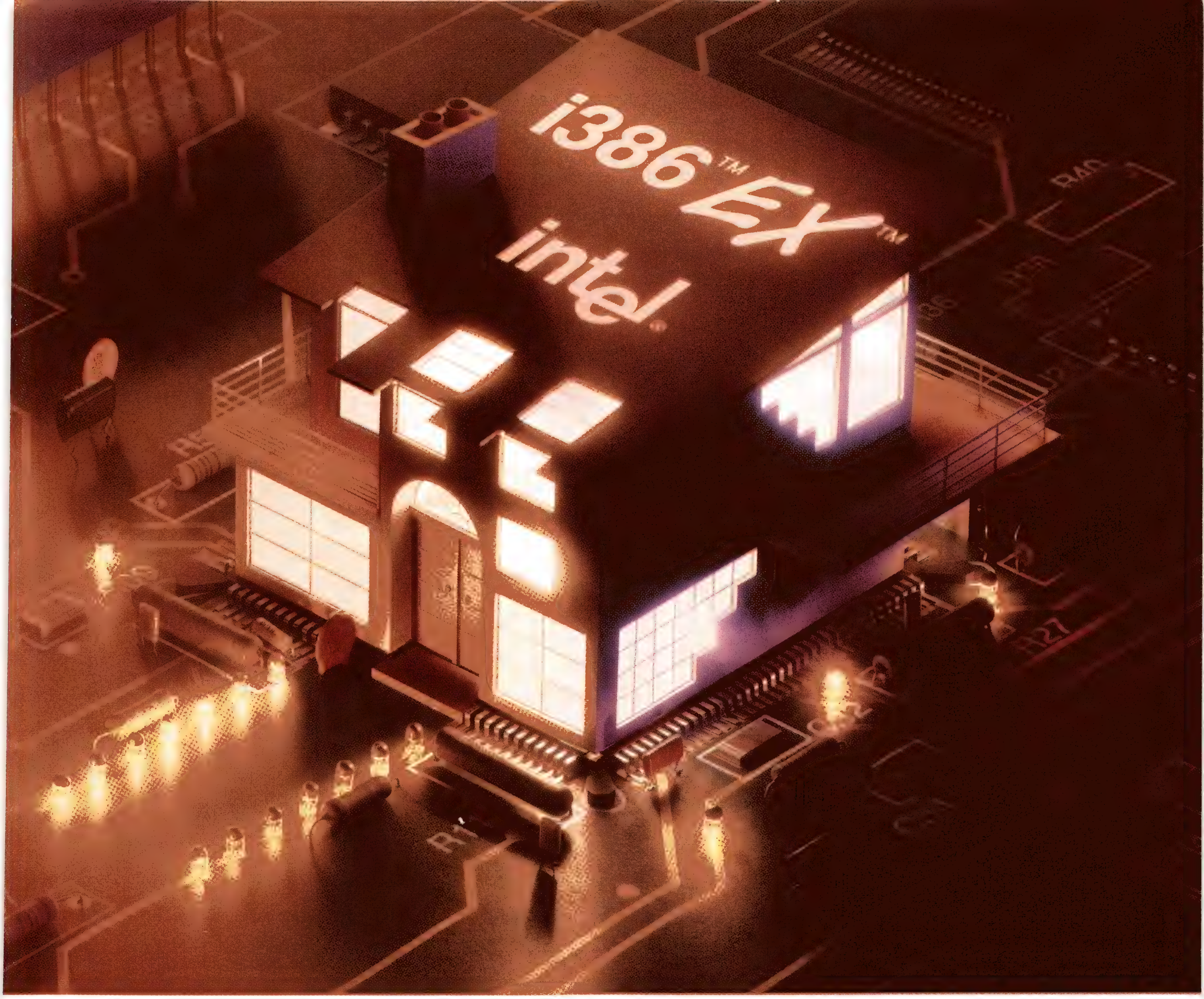

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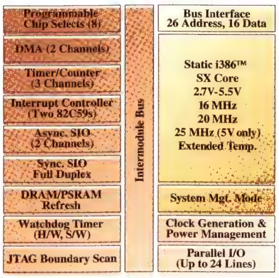
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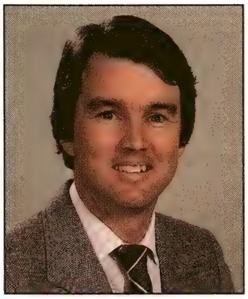
Desktop DOS goes undercover to run embedded systems

DAVID SHEAR, Technical Editor



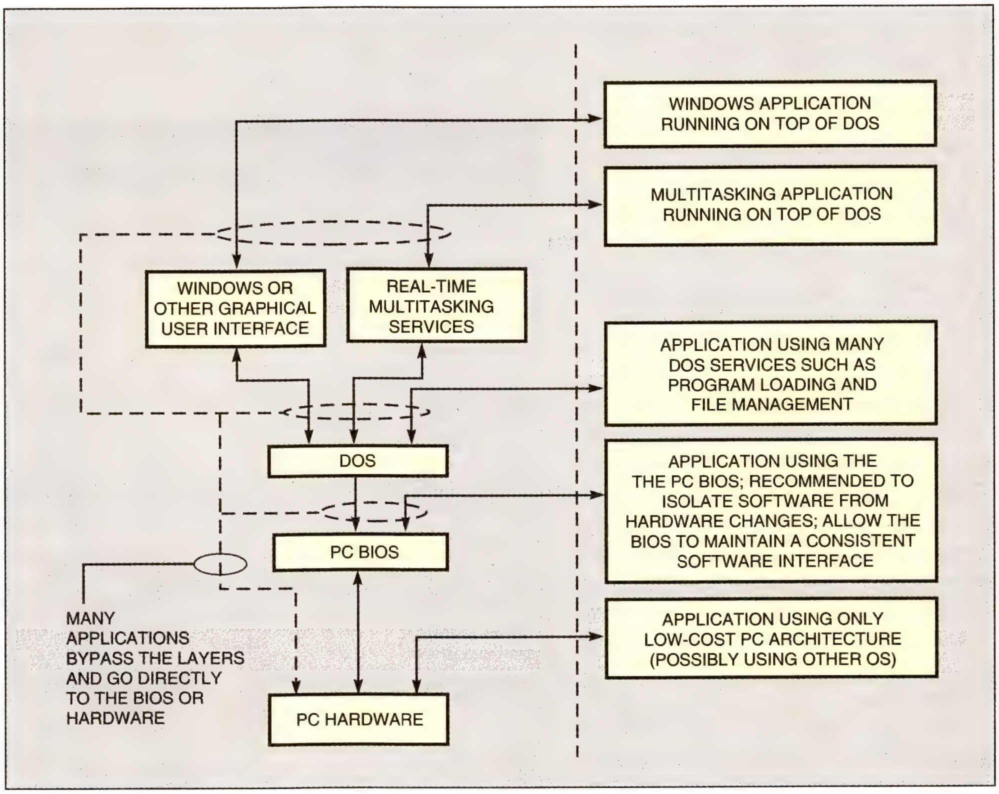
Embedding a PC often involves embedding the most popular desktop operating system.

The PC architecture is continuing its migration to embedded systems. There are many reasons for this migration—as well as some problems this trend has met along the way (**Ref 1**). But cost still tops the list of forces causing a desktop machine's conversion to an embedded system.

The price-performance ratio of embeddable versions of PCs is very attractive. The reduced learning time resulting from using a familiar architecture also tends to lower development cost. You can derive additional savings from the low cost of high-quality tools available in the PC world.

But making a PC work in an embedded environment involves more than just shrinking the hardware. You also need to get your software to run in a system that lacks some of a desktop machine's key components. Many embedded PCs don't have a keyboard, a display, or even a disk drive. They also may not have serial interfaces or a parallel printer port. In fact, without the schematics, it may be impossible to tell that it's a PC.

The embedded PC often runs some version of DOS. Three main players in embedded DOS include Microsoft with MS-DOS ROM, Datalight with ROM-DOS, and General Software with Embedded DOS. Other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PC HARDWARE

Fig 1—This simplified block diagram shows the layers of the PC's software architecture as well as where applications typically interface to it.

versions of "embedded" DOS are Microsoft's MS-DOS, IBM's PC-DOS, or Novell's DR-DOS. You can surround these desktop operating systems (OSs) with tools that ease their implementation in embedded systems.

A DOS-based system provides many services for embedded systems. You can opt for whichever services suit your application. The left side of **Fig 1** shows a simplified block diagram depicting the layers of DOS. To the right of the dashed line are the applications that use the corresponding PC architecture or DOS layer.

One of the most commonly used services is for DOS simply to load a program and then get out of the way, which is not an unreasonable use of the operating system. Standard PC-based tools used to develop programs assume DOS is present. DOS provides system initialization functions; thus, without DOS, the program must initialize the system on its own.

The file-management system is another DOS service frequently used in embedded systems. If you need a file-management system, you certainly could create your own. But why? The DOS file system is adequate for most needs, and creating a file-management system is deceptively complex.

DOS does not directly supply debugging services, but they are available via DOS; for example, you can use Borland's turbo debugger in remote mode. Your PC becomes the keyboard, display, and disks for the embedded system. You can debug your code as if the target had this essential human interface.

Other DOS services are useful in embedded systems. Console I/O and keyboard services can provide a simple user interface. Parallel- and serial-port services can help move data around. Embedded systems often need a time-of-day clock (often battery-backed). Memory-management services within DOS can also be beneficial. Beyond the standard services DOS offers, you can add support for networks, special-purpose boards, and graphical user interfaces (GUI).

DOS does have some disadvantages, specifically that it was never intended for use in embedded systems. But don't underestimate the ingenuity of your peers. It is amazing what DOS has become. One of the biggest obstacles in using DOS in embedded systems is to get it to run without a disk. Running a disk-based OS without a disk requires that the operating system be tricked into thinking that memory is a disk. DOS interprets these solid-state versions of disk drives to be disks. Once the memory assumes the role of a disk, DOS works without change. The memory DOS uses can be RAM, EPROM, or flash ROM, on a board or in a PCMCIA device.

DOS requires memory to run. If your application is severely memory-limited, you may not want valuable resources consumed by something that may provide only a few services.

To drain memory resources even further, a DOS-based system often duplicates your application. It resides on the disk and, when running, resides in RAM. In a diskless system, you need to place your "file" in memory and then have DOS load it into RAM to run. While the application is running, two versions of the application exist. Execute-in-place options exist in versions of DOS intended for embedded use.

DOS is large, but with a few tricks you can make it smaller. For example, if you don't need the rather large COMMAND.COM file, replace it with your application. Then, when the system boots, instead of loading something you don't need, it loads just your program.

DOS has always been a single-threaded OS. Therefore, its developers had no reason to create reentrant services. (A reentrant service is one that more than one task can use at the same time.) For example, if one task is using a service when a higher priority task interrupts it, the service remains available to the higher priority task. Once the higher priority task finishes with the service, the service then reenters and completes without data loss. Many embedded systems require reentrant services, and reentrant versions of DOS are available.

DOS-based systems can also work with real-time systems. DOS itself cannot control your system until your application requests a DOS service. For quick-response needs, you can use the interrupts on the X86 processor.

The only ongoing activity in a DOS-based system is the timer tick, which occurs 18 times/sec. But it doesn't add significant time to interrupt response. Even so, you can disable it because it's needed only for clock and floppy-disk support. Even if you require floppy services, you can still turn it on when you need to access the disk.

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EMBEDDED DOS

The importance of being compatible with MS- or PC-DOS depends on your application. If you are using DOS only to load an application program or for debugging purposes, then compatibility requirements are somewhat soft. On the other hand, if you wish to add networking services, a GUI, and other services, you may find total compatibility with MS- or PC-DOS a requirement.

Another annoyance for the embedded-system developer is that DOS isn't deft at handling errors. When an error occurs, a message appears on the console, and the user must respond via the keyboard. This approach can be somewhat of a problem when the embedded system does not have a console or keyboard, or when you don't want error messages to bother the user.

To work around this, you have to write your own error-handling routines, which isn't too difficult. To check if everything is OK, you can use the libraries that come with most compilers to query a device before you try to use it.

In many cases, the system can't get beyond keyboard testing. Most BIOSs will check for the keyboard and, when not found, ask the operator to press a key to continue. Thus, a system without a keyboard hangs forever. A BIOS for embedded use allows you to start the system without a keyboard.

Another drawback of DOS is that it's rather slow. Using DOS or the BIOS for console I/O, COM-port, and LPT-port operations is not the fastest way to move data. To optimize a system for speed, programmers must use these ports directly. This option takes you to a dangerously low layer by interfacing to the hardware directly. Any change to the hardware requires changes to your application code.

But also realize that, although DOS is slow, the speed of the X86 family of m Ps continues to rise. The price of 386 (and above) m Ps has decreased to the point that simply getting a faster m P is a real solution to the fact that DOS has not been tuned for maximum performance—and it's cheaper in the long run than writing your own optimized code.

Many of the problems associated with using DOS in embedded systems have been addressed with DOS versions that suit embedded systems. Microsoft, Datalight, and General Software have versions of DOS that meet a variety of embedded needs.

Microsoft offers MS-DOS in a form that executes from ROM. These versions are available in developer's kits that include source code for some files so you can customize the OS. Versions 3.22, 3.31, and 5.0 are available in ROM versions. The most popular is Version 5.0, which requires 62 to 115 kbytes of ROM but consumes only about 17 kbytes of RAM.

The ROM versions of MS-DOS are equivalent to the disk-based desktop versions. The ROM versions, however, run out of PROM and treat PROM as a physical drive to eliminate the need for disk drives. The developer's kit allows you to build a PROM image that you can place in EPROM or flash ROM.

MS-DOS is available from either Annabooks (in low volume) or Microsoft (in high volume). Annabooks also sells the MS-DOS Software Developer's Kit for Version 3.xx for $595 and Version 5.0 for $695. Each kit includes 10 licenses.

Microsoft sells only to large-volume accounts. Version 6.22, fully loaded, costs $28/license (10,000). It costs less if you don't need all of the functions. Older versions also cost less.

Datalight's ROM-DOS is compatible with MS-DOS but, from the start, was developed for embedded PROM-based applications. It can boot from either PROM or disk and takes less memory than MS-DOS. (It also costs less.) ROM-DOS 6 has a 45-kbyte kernel and a 27-kbyte command processor. The minimum system takes up 45 kbytes of PROM and 5 kbytes of RAM. To reduce memory requirements further, ROM-DOS works with a royalty-free mini-BIOS that uses just 3 kbytes. It provides only the BIOS services required by ROM-DOS. ROM-DOS also has a miniature version of the command processor, which takes only 4 kbytes.

Another of ROM-DOS' memory-saving options is to create RXE files for programs. RXE files are executable files that can run from PROM. Thus, you avoid duplicating the application. But, for most systems, running from PROM is slower than running from RAM. When you build ROM-DOS, you can choose where to run your application.

To use ROM-DOS, your hardware needs to be based on an 80x86 m P and have RAM and PROM. You can configure ROM-DOS to virtually any hardware within these limitations, even if your BIOS is not 100% PC-compatible. Device drivers making BIOS calls handle all hardware communications. Source code that's also provided lets you modify these drivers to fit your target.

ROM-DOS has been tested with many of the popular DOS applications to verify compatibility. Datalight offers a free demo copy of ROM-DOS so that you can see if it runs with your application.

ROM-DOS is configurable via a build utility; build, a menu-based utility that walks you through the process, automatically configures ROM-DOS for PROM or disk.

ROM-DOS includes a number of utilities, such as remote serial-disk access, which allows a diskless system to access a disk on a desktop machine through a serial port and optional Stacker data compression.

ROM-DOS 6.2 costs $495 for the software developer's kit. It includes all of the development software, Stacker 3.0, a certificate for 20 licenses, and documentation. Additional licenses cost from $25 (for one) and $5 (10,000). ROM-DOS with Stacker costs $40 (for one) and $8 (10,000).

Embedded DOS from General Software goes beyond DOS compatibility; it's actually a real-time, multitasking OS compatible with MS-DOS 3.31. Like other embedded DOSs, it is bootable from PROM or disk. But this version of DOS is built on a preemptive multitasking kernel. It includes 48 services callable from C or assembly language and supports threads, timers, semaphores, and other services.

The file-management services are reentrant. File sharing and record locking are built-in. It supports DOS interrupts 21h through 29h, 2eh, and 2fh and runs .COM and .EXE programs generated with standard MS-DOS development tools. You choose various configuration options to create a desired system. A typical system requires a minimum of 128 kbytes of memory.

Embedded BIOS, a companion product that provides BIOS functions, is also reentrant. With it, you can fit

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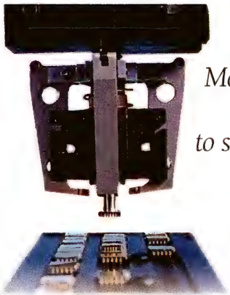

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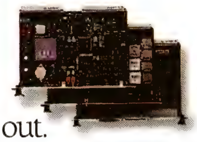

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both Embedded BIOS and Embedded DOS into a single 64-kbyte PROM. Embedded DOS costs $2500 for a full source kit and $995 for a partial source kit. Single licenses cost $10 ($4 for 10,000).

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An example of such a tool is PromKit ($179) from Annabooks. PromKit is a set of programs that allows you to create PROM-based systems. Any file on a disk can be converted into a file residing within PROM. You can load OSs, applications, data files, and libraries into PROM.

This approach to embedding a PC allows you to develop your system on a disk-based desktop PC. Once the application is working properly, you transfer it to a diskless version without code modification. Your application program then loads from PROM just as it loaded from a disk.

PromKit includes a control program, located at an address, that allows the ROM-scan feature of XT- and AT-type machines to operate. This feature checks certain memory locations during the boot sequence; if it finds the appropriate pattern, the boot sequence installs the program. PromKit provides an extension to the normal floppy-disk driver, allowing PROM to replace the physical disk drive.

If you use DOS simply for loading a program, consider not using it at all. A package like C_thru_ROM ($495) from Datalight is a royalty-free product that allows you to take a program developed on the PC and transform it into a standalone application. The output of most DOS-based tools expects that DOS will be there to set up the system and allow the program to run. Without DOS, your application must initialize the system itself. These tools provide initialization and other services to let you place your program into PROM.

The ongoing flood of consumer products from the PC world continues to attract attention from embedded-system developers. It's difficult to ignore low-cost, high-quality tools—and the hardware's tremendous bang for the buck. As more people consider the PC for embedded systems, it will only get easier to use these products. EDN

Reference

1. Shear, David, "Embedded systems developers embrace the PC architecture," *EDN*, March 3, 1994, pg 39.

You can reach Technical Editor David Shear at (503) 754- 9310; fax (503) 758-9242.

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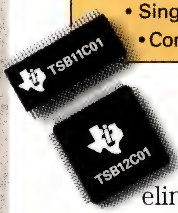

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NEC launches high-volume production of x8 and x16 devices

Byte-wide 16M DRAMs are just about to reach the cost-per-bit crossover point. They already save space and equal or surpass 4M devices in every meaningful specification.

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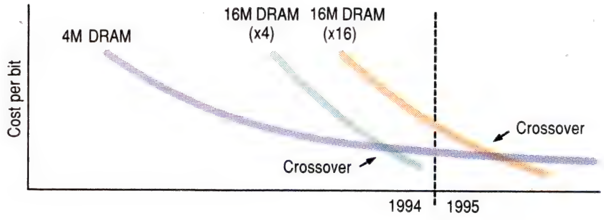

Byte-wide 16M DRAMs have the most efficient organizations for PC and workstation memories. Now is the time to make sure your system is ready to use these advanced devices. And to meet your volume and variety needs, NEC is

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rapidly expanding production capacity.

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For designers of PCs and workstations, it's time to switch to byte-wide 16M DRAMs. NEC has the volume, variety and production capacity you need.

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Organization	Voltage	Speed (ns)	Refresh	Functions	Package
2M x 8	5.0V 3.3V	50, 60, 70, 80 (5.0V) 60, 70, 80 (3.3V)	4K/2K	Fast Page Hyper Page	TSOP II SOJ
1M x 16			4K/1K		

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CIRCLE NO. 115

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MCM6729A*	MCM6706A	MCM6705A	MCM6708A
256K x 4 bit	32K x 8 bit	32K x 9 bit	64K x 4 bit
8, 10, 12, 15ns	8, 10, 12ns	10, 12ns	8, 10, 12ns
MCM6709A*	MCM6706R	MCM6709R	
64K x 4 bit	32K x 8 bit	64K x 4 bit	
8, 10, 12ns	6, 7, 8ns	6, 7, 8ns	

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☐ 12ns

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SYNCHRONOUS MEMORIES

As system clock speeds push past 50 MHz, designers are discovering that asynchronous memory becomes unmanageable. As a result, they are looking to synchronous memories to handle increasing system speeds. What they are finding are new design challenges.

Two trends in advanced processor design have converged to establish a need for new memory interfaces. One trend is the increase in CPU clock speed to 66 MHz and beyond. The other is the integration of primary cache memory into the processor die. This convergence resulted in systems that make high-speed burst demands from their main memory. Synchronous memories emerged to meet those demands, but you can't treat them like commodity memories.

Synchronous memories provide high-speed operation by latching incoming address, data, and control signals into on-chip registers. The act of latching these signals decouples the processor's addressing cycles from the memory's access cycle, freeing the two to operate in parallel rather than having to wait for one another. The parallelism collapses the overall duration of a memory burst access, speeding system operation.

Rather than sit and hold address lines steady, for example, the processor can initiate a second memory request before the memory device has responded to the first. This early initia-

RICHARD A QUINNELL, TECHNICAL EDITOR

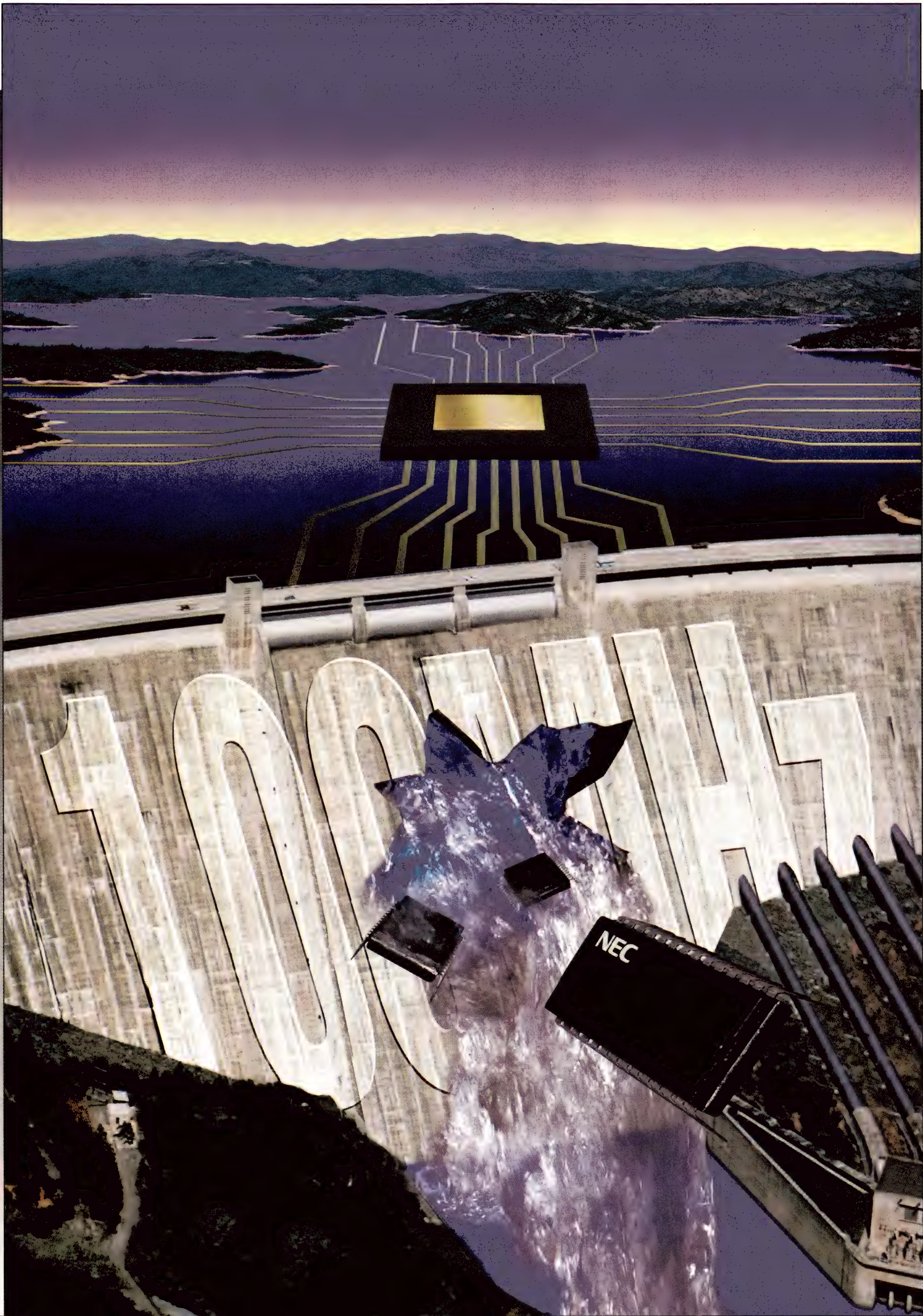


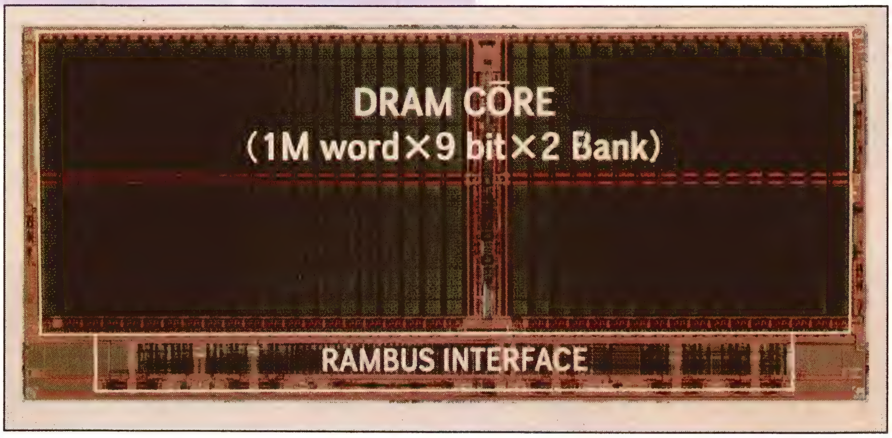
Photo courtesy NEC Electronics Inc

tion is especially noticeable during write cycles. The processor doesn't need to hold its output lines steady during the memory's write cycle. It only needs to present the data at the clock edge, then it's free to prepare for its next task while the memory completes the transaction.

When synchronous memories use a pipeline architecture (that is, they have registers for output signals as well as input signals) they produce additional performance gains. In a pipelined device, the internal memory array needs only to present its data to an internal register to be latched rather than pushing the data off the chip to the rest of the system. Because the array only sees the internal delays, it presents data to the latch faster than it would if it had to drive off chip. Further, once the latch captures the array's data, the array can start preparing for the next memory cycle while the latch drives the rest of the system.

With the latches holding information and freeing other elements of the memory subsystem to prepare for the next access cycle, synchronous memories shave several nanoseconds off the overall memory cycle time. Manufacturers, therefore, can produce synchronous memories that are more than 20% faster than asynchronous memories built with the same process. A 12-nsec SRAM process, for example, will produce 100-MHz synchronous SRAMs (SSRAMs).

A synchronous memory interface can also simplify memory control design. Asynchronous memories depend on properly timed and shaped pulses on their control lines. With total cycle times approaching 10 nsec (for 100-MHz systems), the pulse shape becomes increasingly intolerant of error, and therefore, harder to design. Synchronous memories avoid the need for critical pulse shapes, depending only on the placement of clock edges relative to the other data, often using the same clock as the rest of the system.

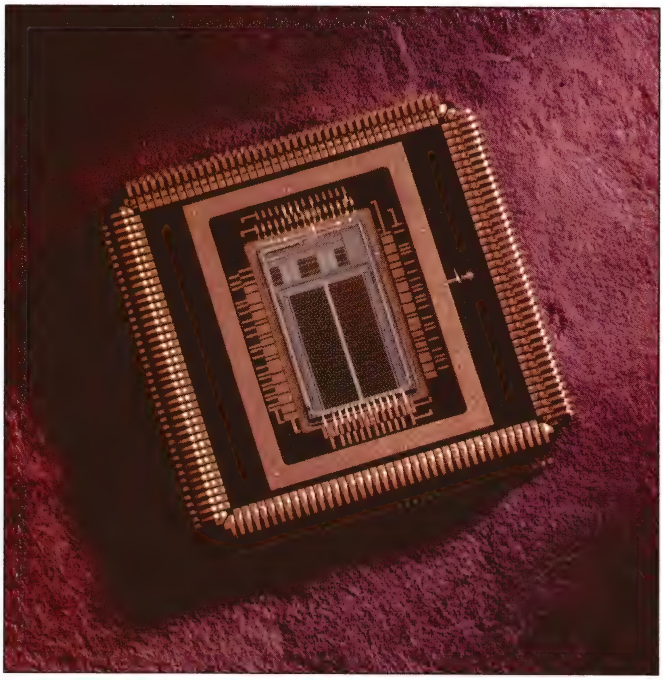


Combining a novel interface structure with a DRAM core, the Rambus DRAM is able to achieve a 500-Mbyte/sec data burst rate. The Rambus interface is synchronous to a 250-MHz clock. (Photo courtesy of NEC)

Three major synchronous versions of traditional memory types have arisen over the last two years: SSRAMs, synchronous DRAMs (SDRAMs), and synchronous FIFOs. Unfortunately for designers, few standards for synchronous-memory operation exist, and the devices offered by various manufacturers often differ considerably. Even where standards exist, manufacturers have added their own enhancements to the standard to give their devices a market advantage. These differences complicate the task of finding multiple sources of compatible parts.

There are several variations of the SSRAM, for example, as shown in **Table 1**. Some devices, such as the Cypress CY7C193, provide just the basic elements of an SSRAM: latches for address and data inputs. Many other SSRAMs incorporate a burst-mode counter, allowing the processor to retrieve four or more consecutive words in rapid succession. The burst-counter circuitry in the memory device speeds system operation by eliminating the delays associated with propagating burst-address information from the memory controller to the memory. The memory device thus begins its access cycle as soon as the clock edge occurs rather than waiting several nanoseconds for the address to arrive and stabilize. As a result, a burst-mode memory in a 50-MHz system can function with a 13-nsec access time. A nonburst device would need a 7-nsec access time.

Among the SSRAMs with burst counters there are further variations. Some SSRAMs, such as the NEC μPD431432, produce a linear addressing sequence (1-2-3-0) during the burst operation, matching the needs of



Cache DRAMs are among the specialty synchronous memories that handle rising system speeds. This device from Sony works at 50 MHz and matches the burst demands of the 80486 processor.

TABLE 1—SYNCHRONOUS SRAMs

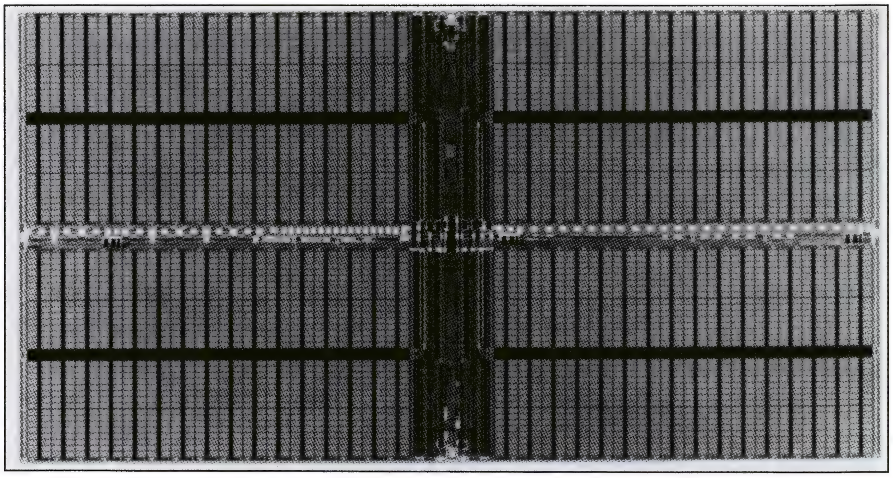
Company	Part no.	Size (bits)	Clock rate (MHz)	Access time[1]		Burst mode[2]	Price (1000)[3]	Comments
				Pipeline	Nonpipeline			
Cypress **Circle No. 326**	CY7C193	32k×8	33		20		$3.50	
Fujitsu **Circle No. 327**	MBVP036	32k×36	66	1		S	N/A	Available in the fourth quarter.
	MBVT036	32k×35	66		8	S	N/A	Available in the fourth quarter.
Hitachi **Circle No. 328**	HM67A4257	256k×4	100	1			$40	
	HM67A4101	1M×4	100	1			$175	
	HM67B1864	64k×18	66		9	I, L	$50	Burst mode is a mask option.
	HM67B3632	32k×36	66		9	I, L	$50	Burst mode is a mask option.
IDT **Circle No. 329**	IDT71V432	32k×32	66		9	I	$20	
	IDT71420	32k×18	66		9	I	$30	
	IDT71419	32k×18	66		9	L	$30	
Micron **Circle No. 330**	MT58LC32K36B2	32k×36	66		9	S	$45	
	MT58LC32K32B2	32k×32	66		9	S	$45	
	MT58LC64K18B2	64k×18	66		9	S	$45	
	MT58LC32K36C4	32k×36	125	2		S	$45	
	MT58LC32K32C4	32k×32	125	2		S	$45	
	MT58LC64K18C4	64k×18	125	2		S	$45	
Motorola **Circle No. 332**	MCM62973A	4k×12	50	2			$13.50	
	MCM62974A	4k×12	55	2			$13.50	Output enable
	MCM62975A	4k×12	40	2	10		$13.50	Output enable, transparent latch.
	MCM67D709	128k×9	100		5+1 clock		$79	Dual data ports.
	MCM67Q709	128k×9	100		5+1 clock		$79	Separate input and output ports.
	MCM67Q804	128k×9	100	2			$79	
	MCM62110	32k×9	66	1			$29.60	Dual data ports.
	MCM62486	32k×9	66		11	I	$19.43	
	MCM62940	32k×9	66		11	L	$19.43	
	MCM62980	64k×4	66		15		$28	
	MCM62981	64k×4	66		15		$28	Bit write.
	MCM62990A	16k×16	66		12		$15.90	
	MCM67B518	32k×18	66		9	I	$26.95	
	MCM67H518	32k×18	66		9	I	$26.95	
	MCM67M518	32k×18	80		9	L	$26.95	
	MCM67C518	32k×18	66	2		I	$26.95	
	MCM67J518	32k×18	66	2		I	$26.95	
	MCM67B618	64k×18	66		9	I	$55	
	MCM67H618	64k×18	66		9	I	$55	
	MCM67M618	64k×18	80		9	L	$55	
	MCM67C618	64k×18	66	2		I	$55	
	MCM67J618	64k×18	66	2		I	$55	
NEC **Circle No. 333**	µPD431432	32k×32	66		9	L	$50	
	µPD431232	32k×32	66		9	I	$50	
Paradigm **Circle No. 334**	PDM44528	32k×18	66		9	I	$41	
	PDM44538	32k×18	66		9	L	$41	
	PDM44259	32k×9	66		9	I	$47	
	PDM44659	32k×9	66		9	L	$47	
	PDM44018	64k×18	66		9	I	$60	Pipeline mode is an option.
	PDM44038	64k×18	66		9	L	$60	Pipeline mode is an option.
	PDM44028	64k×18	66		9	I	$60	Pipeline mode is an option.
Samsung **Circle No. 338**	KM741006	256k×4	100		6.5		$60	
	KM718B86	64k×18	66		9	I	$50	
	KM718B91	64k×18	66		9	L	$55	
	KM718BV87	64k×18	66		9	I	$50	3.3V.
	KM732V588	32k×32	75	2		I	$25	3.3V.
	KM732V592	32k×32	75	2		L	$25	3.3V.
SGS-Thomson **Circle No. 339**	MK62486	32k×9	40		19	I	$8.39	
	M62486A	32k×9	66		11	I	$14.64	
	M62486B	32k×9	50		11	I	$9.84	
	M62486AR	32k×9	66	2		I	$16.10	
	M62486BR	32k×9	50	2		I	$13.31	
	M67B618	64k×18	66		9	I	$53.24	
	M67H618	64k×18	66		9	I	$53.24	
	M67C618	64k×18	66	2		I	$58.56	
	M67J618	64k×18	66	2		I	$58.56	
	M67P618	64k×18	66	2		I	$58.56	
Sony **Circle No. 341**	CXK77920	262k×9	90	2			$120	
	CXK77910	128k×9	100	2			$60	TSOP, SOJ, mirror packages.
	CXK77410	256k×4	100	2			$57.10	Separate input and output ports.
Toshiba **Circle No. 343**	TC55BS4258	256k×4	100		5+1 clock		$67	Separate input and output ports.
	TC55BS8125	128k×8	100		5+1 clock		$67	
	TC55BS8128	128k×8	100		5+1 clock		$67	Separate input and output ports.

Notes: 1. Access time for pipelined devices is in clock cycles. For nonpipeline devices access time is in nsec clock-to-data.
2. Burst mode: I=Interleaved (Intel), L=Linear (Motorola), S=pin selectable.
3. Price is as of April 15, 1994, or date of introduction for the fastest speed grade.

▶ **Super Circle Number 344**

the PowerPC and 68040 processors. Others, like the NEC µPD431232, produce an interleaved address sequence (1-0-3-2) to match the Pentium and 80486 burst sequence. Some devices, like the Samsung KM44S4020A, allow you to select the sequence. There are also pipelined and nonpipelined varieties.

Pipelined devices use a latch on the output lines, adding a 1-clock delay or latency to retrieval of the first word in a burst read. As with the input signal latches, however, the output latch frees the circuits preceding it to begin a new cycle, saving time for the next access. Memory vendors report that the same process that produces a marginal (20% yield) 66-MHz nonpipelined SSRAM will easily provide a 75-MHz pipelined version.



To fit this synchronous DRAM's 64-Mbit 4-bank memory array along with its burst counter and pipeline registers into a narrow package, Fujitsu moved the device's I/O pads to the die's center.

Unlike SSRAMs, SDRAMs have a JEDEC standard to follow. Not all of them follow it, however. The major difference between standard and nonstandard SDRAMs occurs in the use of the RAS (row address select) line. In JEDEC-standard SDRAMs, RAS and other control signals form an operating code that gets sampled on the rising edge of the clock, then the control signals are no longer needed. Supplying first a row address and then a column address to the SDRAM results in the RAS signal being asserted for only one clock cycle, ie, the RAS signal occurs as a pulse.

To mimic the operation of conventional DRAMs, however, some SDRAM vendors chose a level-RAS signal scheme. Conventional page-mode

TABLE 2—SYNCHRONOUS DRAMs

Company	Part no.	Size (bits)	Clock rate (MHz)	Latency[1] (cycles)[2]	Price (1000)	Comments[3]
Fujitsu **Circle No. 327**	MB81116420	2×2M×4	100	P	N/A	Dual bank, available in the third quarter.
	MB81116820	2×1M×8	100	P	N/A	Dual bank, available in the third quarter.
	MB81164840	4×2M×8	100	P	N/A	Four bank, available in the fourth quarter.
	MB81141620	256k×16	100	P	N/A	Available in the fourth quarter.
Hitachi **Circle No. 328**	HM5241605	256k×16	80	3	$29	Full-page burst.
	HM5216800	2M×8	80	3	N/A	Full-page burst, available 2nd quarter of 1995.
	HM5283206	256k×32	80	3	N/A	Optimized for graphics, with block right mask, also, 3.3V, available in the second quarter, 1995.
Mitsubishi **Circle No. 331**	M5M4V16407	4M×4	100	P	$75	
NEC **Circle No. 333**	µPD4516421G5	4M×4	100	P	$155	Full-page burst, 3.3V.
	µPD4216161G5	1M×16	100	P	$193	Full-page burst, 3.3V.
	µPD4216821G5	2M×8	100	P	$193	Full-page burst, 3.3V.
Samsung **Circle No. 338**	KM44S4020A	4M×4	100	3	$94	3.3V.
			66	2	$81	3.3V.
			33	1	$81	3.3V.
	KM48S2020A	2M×8	100	3	$94	3.3V.
			66	2	$81	3.3V.
			33	1	$81	3.3V.
Texas Instruments **Circle No. 342**	TMS626402	2M×4×2	80	P	$129	Dual bank.
	TMS626802	1M×8×2	100	P	$129	Dual bank.
Toshiba **Circle No. 343**	TC59S1604FT	4M×4	100	2	N/A	Available in the third quarter.
	TC59S1608FT	2M×8	100	2	N/A	Available in the third quarter.

Notes:
1. Latency is CAS-to-data-valid, P=programmable.
2. Price is as of April 15, 1994, or date of introduction for fastest speed available.
3. JEDEC standards include programmable burst length of 1, 2, or 4 words and programmable burst mode.

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DRAMs require that RAS remain asserted throughout a burst. The level-RAS mimicry allows conventional DRAM-controller designs to work with the non-JEDEC SDRAM devices. The controllers would not work properly with JEDEC-standard SDRAMs.

Experience with conventional DRAMs suggests that SDRAMs conforming to the JEDEC standard would be compatible. Unfortunately, there are still architectural variations within the standard. Some devices have dual internal memory banks, allowing them to fetch data from two consecutive addresses simultaneously, then present them in succession to the output buffers. An alternative design uses internal pipelining to retrieve the next data word from the internal array while the device presents the first word to the outside. The pipelined devices offer only a single array.

The difference between the two architectures is transparent to the user during normal burst reads. If the burst gets interrupted, however, and memory access resumes at a new column address, the prefetch design requires a 1-clock delay before changing column addresses. The pipelined design can respond immediately. To accommodate both architectures, the JEDEC standard requires that designers allow 2n clocks between address cycles when changing column addresses within the same row. Following this rule ensures that both architectures behave the same in your design, but it sacrifices the performance advantages of the pipelined memory. **Table 2** summarizes the various SDRAMs available.

TABLE 3—RAMBUS DRAMs

Company	Part no.	Size (bits)	Price (1000)
NEC **Circle No. 333**	µPD488130 µPD488170	2M×8 2M×9	$200 $230
Toshiba **Circle No. 343**	TC59R0409 TC59R1609	512k×9 2M×9	* *

Notes: RDRAMs use a 250-MHz clock, shifting data on each edge. A read access has a 14-clock latency.

*Available in the fourth quarter

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In addition to the internal architectural differences, JEDEC-standard SDRAMs from different manufacturers offer different options. Manufacturers have added proprietary features to their "JEDEC-standard" devices to better match special applications. One such feature is the ability to perform a full-page burst length in addition to the standard 4-word burst. The standard encompasses such special features by reserving the control-signal codes that activate the added features. Thus, devices with and without the feature can meet the standard. Therefore, if you want to use such superset features, make sure all your SDRAM suppliers offer the same feature set. JEDEC compliance is no assurance that they do.

One novel synchronous DRAM that doesn't resemble the JEDEC standard, yet is fully standardized, comes from Rambus Inc and its licensees. The Rambus DRAM (RDRAM) achieves a blazing 500-MHz burst data-transfer rate. When accessed, it holds data from an entire column of the memory array in its sense amplifiers, using the amplifiers as an on-chip cache. The device then can produce a data burst beginning at any place within the column. The data comes sequentially over a controlled-impedance bus, one data word on each

MANUFACTURERS OF SYNCHRONOUS MEMORIES

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edge of a 250-MHz clock. Rambus has fully defined the memory's operation, access protocols, pinout, and interchip bus design in order to ensure that RDRAMs from various manufacturers will be compatible. A list of RDRAM devices currently available appears in **Table 3**.

Rambus also developed a memory-controller design to simplify RDRAM use in systems. That controller design has been available in ASIC libraries. Now, it is beginning to emerge in standard products. NEC, for example, has incorporated the RDRAM interface in its memory controller for the V_R4400-series MIPS processor. RDRAM-compatible memory controllers for PCI graphics chipsets are due out in late 1994 and early 1995. Controllers for Pentium main memory are also in the works and expected by mid-1995.

FIFOs are the third memory type that speed demands have driven to synchronous operation. At first glance, conventional FIFOs already seem synchronous in nature, using strobes to clock data in and out. However, these strobes use both edges, with each edge triggering a different internal operation. Further, status signals such as Data Ready and Full are asynchronous and occur as soon as propagation delays allow. At high clock speeds, the necessary control signals become increasingly difficult to produce within tolerances.

Asynchronous FIFOs have another difficulty at high speed: They suffer from operational problems at certain combinations of input and output clock frequencies. Flags could appear just as data strobes occurred, resulting in lost data. Worse, the flag circuitry could enter a metastable state if set by one port's data strobe just before being reset by the other port's strobe. As a result, the flags lines could display erroneous status information. Synchronous interfaces in FIFOs, then, serve to boost reliability as well as speed.

Synchronous FIFOs solve the lost-data problem by aligning flag signals to the port's data clock and by providing data buffers to hold information pending system recognition of the FIFO's status. However, metastability still remains a possibility for flag signals. To solve that problem, manufacturers such as Texas Instruments, IDT, and Quality Semiconductor began double-registering the flag signals to give a full clock period for a metastable flag to resolve itself before the FIFO presents that flag to the outside world.

Such double-registered FIFOs are called clocked FIFOs to distinguish them from synchronous FIFOs with only single registering. The timing of their flags can differ from other synchronous FIFOs, so you need know with which type you're dealing. A summary of synchronous FIFOs appears in **Table 4**.

Clocked FIFOs also offer first-word fall-through, meaning that the first word entered into the FIFO is available at the output lines at the same time that Data Ready goes true. Other FIFOs present the flag first, making data available only after the first Read clock. An awareness of this difference will prevent losing that first word

TABLE 4—SYNCHRONOUS FIFOs

Company	Part no.	Size (bits)	Clock rate (MHz)	Price[1] (1000)	Comments
IDT **Circle No. 329**	72420/1	64×8/9	83.3	$21.10	
	72200/1	256×8/9	83.3	$21.10	
	72210/1	512×8/9	83.3	$24.25	
	72220/1	1k×8/9	66.7	$27.10	
	72230/1	2k×8/9	66.7	$41.90	
	72240/1	4k×8/9	66.7	$58.80	
	72205	256×8	66.7	$35	
	72215	512×18	66.7	$40.65	
	72225	1k×18	66.7	$51.30	
	72235	2k×18	66.7	$83.90	
	72245	4k×18	66.7	$112.50	
	72801	256×9	66.7	$31.20	Dual bank.
	72811	512×9	66.7	$35.80	Dual bank.
	72821	1k×9	50	$40.20	Dual bank.
	72831	2k×9	50	$60.30	Dual bank.
	72841	4k×9	50	$90.70	Dual bank.
	72605	256×18×2	50	$54.80	Bidirectional.
	72615	512×18×2	50	$87.80	Bidirectional.
	723632	512×36×2	67	$96.20	Bidirectional.
	723641	1k×36	67	$109	
Mitsubishi **Circle No. 331**	M66250	5k×8	20	$20	Works as FIFO or LIFO.
	M66251	5k×8	25	$7.25	
	M66252	1152×8	20	$6.50	
	M66253	5k×8×2	25	$20	Dual bank.
Paradigm **Circle No. 334**	PDM42205	256×18	100	$44	
	PDM42215	512×18	100	$51	
	PDM42225	1k×18	100	$64	
	PDM42235	2k×18	100	$95	
	PDM42245	4k×18	100	$150	
Quality **Circle No. 335**	QS7244A	4k×9	66	$36	Clocked.
	QS723661	4k×36	50	$84	Clocked.
	QS7230HD	64k×9	66	$9	Clocked.
Sharp **Circle No. 340**	LH5492	4k×9	40	$25.60	Clocked.
	LH540215	512×18	50	$25.60	Clocked.
	LH540225	1k×18	50	$30.40	Clocked.
	LH5420	256×36×2	40	$56	Clocked, bidirectional.
	LH543620	1k×36	50	$60	Clocked.
Texas Instruments **Circle No. 342**	SN74ABT3611	64×36	67	$30	Clocked.
	SN74ABT3612	64×32×2	67	$40.53	Clocked, bidirectional.
	SN74ABT3613	64×36	67	$32.11	Clocked.
	SN74ABT3614	64×36×2	67	$46.84	Clocked, bidirectional.
	SN74ABT7819	512×18×2	83	$63.13	Clocked, bidirectional.
	SN74ABT3632	512×36×2	67	$78.95	Clocked, bidirectional.
	SN74ABT3638	512×32×2	67	$73.68	Clocked, bidirectional.
	SN74ABT3641	1k×36	67	$84.21	Clocked.
	SN74ABT7803	512×18	67	$31.26	Clocked.
	SN74ABT7805	256×18	67	$25.91	Clocked.
	SN74ABT7807	2k×9	67	$31.58	Clocked.

Note: 1. Price is as of April 15, 1994, or date of introduction for fastest speed available.

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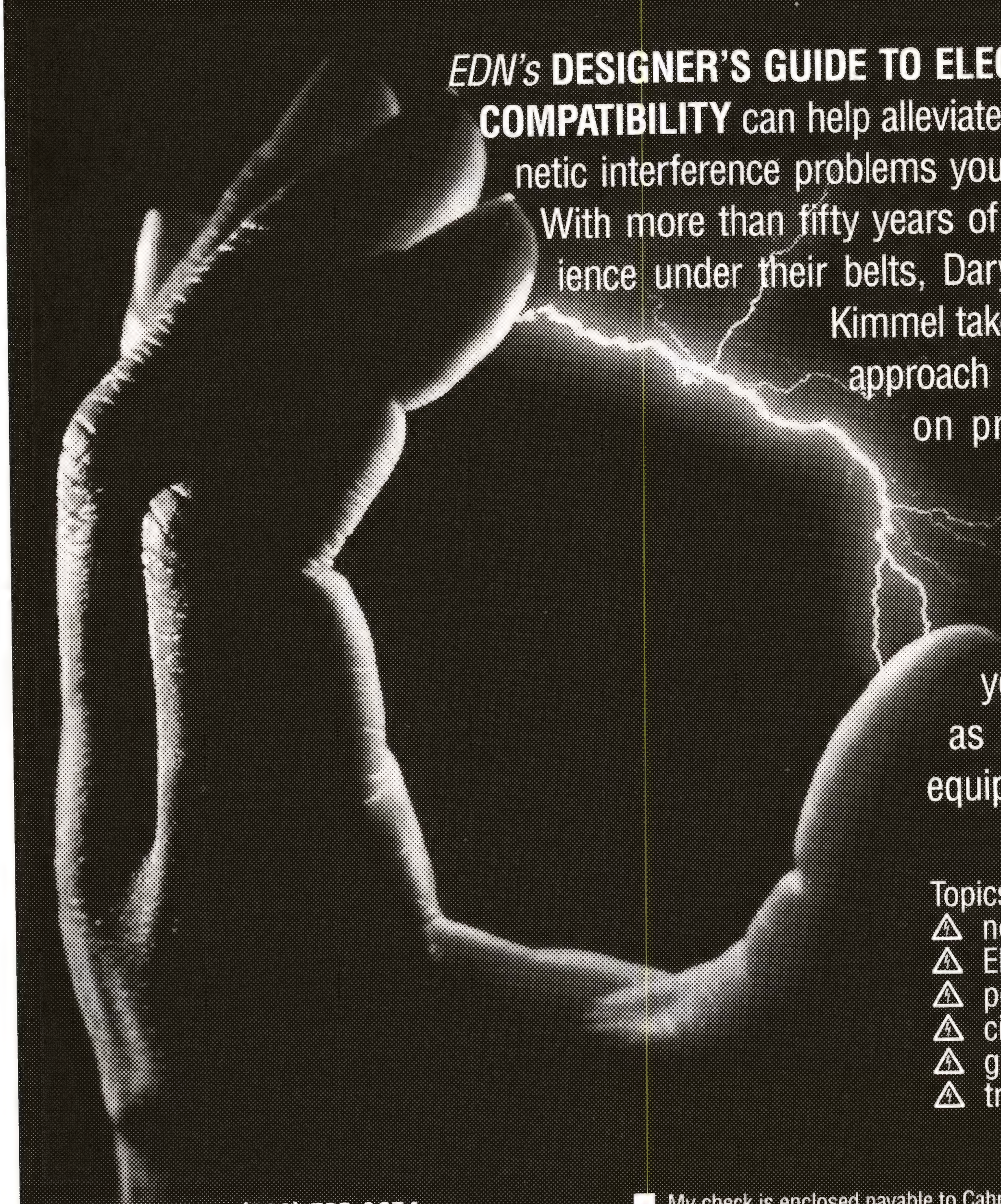

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when reading from a clocked FIFO.

A handful of other memory types with synchronous interfaces exist; all are designed to speed the system's access to the memory array. These include PROMs, cache DRAMs, and enhanced DRAMs. As shown in **Table 5**, these additional memory types are not widely offered. Such devices meet the needs of unique applications and do not reflect the main industry trend toward synchronous memories.

Synchronous-memory cost premium

All the variations within the main trend present a challenge if you're looking for multiple supply sources. If your design uses the special features of some SDRAMs, for example, you may have fewer alternatives than if you're following JEDEC standards. You will need to check carefully to see which parts are compatible with your application.

The wide variation among synchronous memories also affects their cost. The devices serve many niche applications rather than one large common application. Without the production volume generated by a large application, costs for synchronous memories include a premium that is relative to other memories. That premium now sits at 20 to 50% over the cost of a comparable asynchronous part and is unlikely to vanish completely.

Even if vendors converge on a standard feature set and production volumes skyrocket, synchronous memories will still carry a cost premium. High-volume production was expected to eventually reduce the synchronous memory premium to 5%, but manufacturers are discovering that non-pipelined memory devices suffer poor production yields in the higher speed grades. Further, the added die size of pipelined designs and the cost of test-

TABLE 5—OTHER SYNCHRONOUS MEMORIES

Company	Part no.	Type	Size (bits)	Clock rate (MHz)	Price[1] (1000)	Comments
Cypress **Circle No. 326**	CY7C225A	PROM	512×8	33	$6.25	
	CY7C235A	PROM	1k×8	33	$12.20	
	CY7C245A	PROM	2k×8	40	$12.05	
	CY7C265	PROM	8k×8	37	$25.45	
	CY7C277	PROM	32k×8	22	$48.05	
	CY7C287	PROM	64k×8	16.7	$51.35	
	CY7C25819	PROM	2k×16	100	$28.80	
	CY7C249	PROM	2k×16	55.6	$21.55	
IDT **Circle No. 329**	IDT71215	Cache tag	16k×15	66	$18	
	IDT71216	Cache tag	16k×15	66	$18	
	7099	Dual port	4k×9	50	$38.90	
	70825	Dual port	8k×16	33	$45.45	
	20824	Dual port	4k×16	33	$32.46	
Mitsubishi **Circle No. 331**	M5M4V4169TP	Cache DRAM	256×16	66	$17.50	
	M5M4V16169TP	Cache DRAM	1M×16	100	$68.80	
Motorola **Circle No. 332**	MCM62X308	Line buffer	8k×8	33	$4.46	
	MCM62Y308	Line buffer	8k×8	50	$4.46	
	MCM62981	Line buffer	64k×4	66	$28	Bit write.
Ramtron **Circle No. 337**	DM2223	Cache DRAM	512k×8	66	$19.53	Burst mode.
Sony **Circle No. 341**	CXK784862Q	Cache SRAM	32k×36×2	33	$121.40	
	CXK784862Q	Cache SRAM	32k×36×2	50	$139.60	

Note: 1. Price is as of April 15, 1994, or date of introduction for highest speed grade.

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LOOKING AHEAD

Synchronous memories are presently in use in applications requiring the highest performance, regardless of cost. They have the potential of becoming a mainstream memory, however. Systems operating above 50 MHz become extremely difficult to design using asynchronous memories.

The problem is that manufacturers developed their synchronous memories to meet the needs of specific customers, and then offered the memories as standard products. The resulting confusion of feature sets and memory types has intimidated most mainstream memory system designers and kept prices at a premium due to low-production volume. Mainstream memory designers are fairly conservative and are waiting for prices to drop and standards to emerge.

Both events are likely to occur over the next one and a half to two years. The factor that will force the issue is system clock rates. Workstation designs are already beginning to include synchronous memories to meet their performance needs. By 1995, most new workstations will use synchronous memory. Mainstream PCs will probably follow suit two to three years later as entry-level PCs push the 50-MHz-clock mark.

In the meantime, vendors are cross-licensing their synchronous memory designs and developing new standards to address user concerns about multiple sources. Vendors are also converging on a common feature set, so that the next generation of synchronous memories will look more homogeneous than these early devices. Those activities will also begin to bear fruit by 1995.

At that point, asynchronous memories may begin to fade away. Already Fujitsu has declared that it expects SDRAM to become the next commodity memory and will not be developing another generation of asynchronous DRAM. Other companies, however, estimate that SDRAM will meet only 40% of the market's main-memory needs. Either way, the implication is clear: Synchronous memories will become a staple of the designer's kitchen for preparing systems in the coming years.

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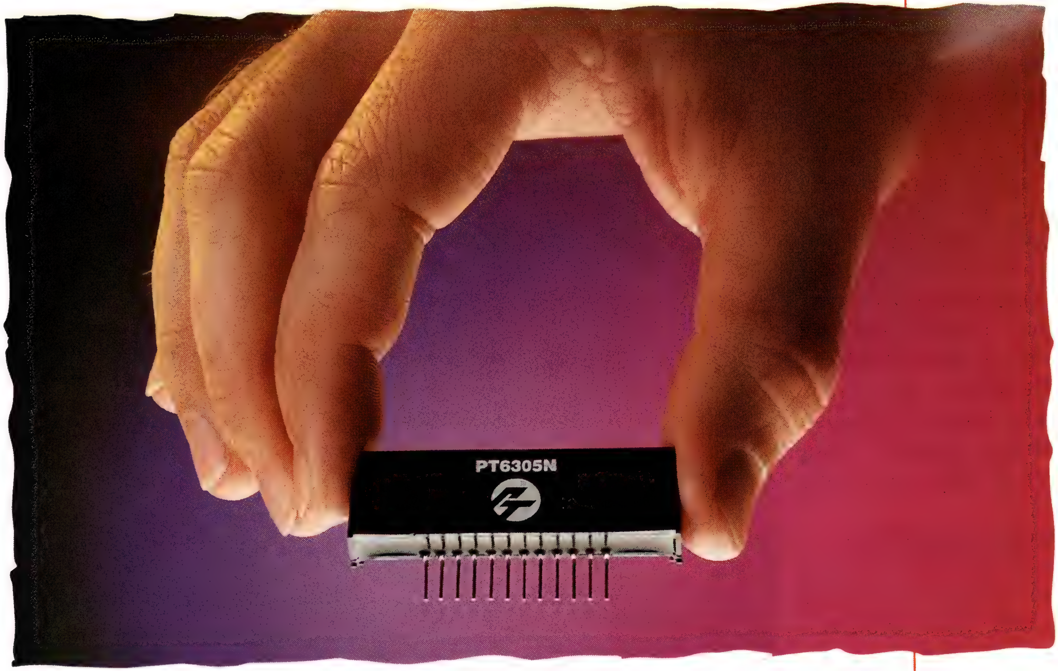

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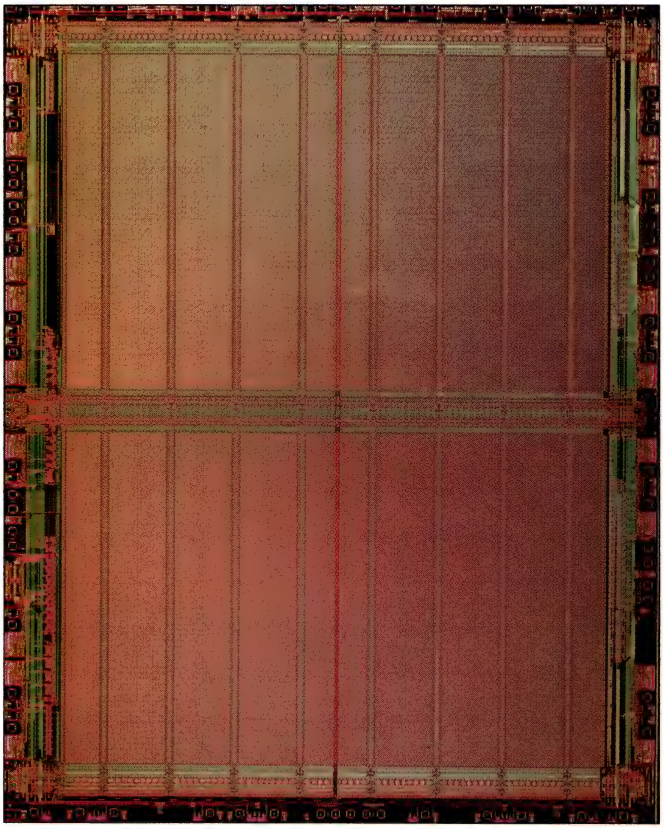
ing high-speed parts are working to keep that premium high. Most manufacturers acknowledge that synchronous memories will carry a 20% premium for the foreseeable future.


The burst counter and registers on the sides of this 1-Mbit synchronous SRAM from Motorola exact only a small die-area penalty. Low demand and testing costs account for most of the cost premium such devices have over their asynchronous counterparts.

Some of those premium costs can be offset in the rest of your system by the design simplification that results from using synchronous memories. Instead of having to produce carefully shaped pulses without a clock reference, controllers for synchronous memories can use the same clock as the CPU bus. Designers must still take care, however, because new timing concerns arise with synchronous memories.

Synchronous interfaces

One timing concern you need to be aware of is the setup and hold requirements of the memory's address and data input lines. Many synchronous memories, for example, need address and data stable 2.5 nsec before the system clock. You need to be sure that the processor's output signal timing matches the memory's needs, or you may miss a cycle during memory access. For the same reason, pay attention to clock skew in large blocks of memory to ensure that all memory blocks behave the same.

Another timing concern new to synchronous memories is a tight requirement on the clock duty cycle. The μPD4516421 from NEC, for example, specifies a minimum clock high of 3.5 nsec and a minimum clock low of 3.5 nsec for a 100-MHz cycle time. Those specifications allow a ±15%-duty cycle variation. Because most logic buffers have a different propagation delay for low-to-high transitions than for high-to-low ones, you'll need to take care to ensure that your clock-distribution scheme doesn't erode the clock's duty cycle.

If you want to use synchronous memory, you may find that you have to design your own memory controller. Standard memory controllers, including those built into processor chip sets, generally assume an asynchronous memory. The few that do handle synchronous memories may not work with pipelined devices.

Perhaps the single most limiting factor in the use of synchronous memories, however, is that they are designed for specific applications. SSRAMs, for instance, are designed to serve as secondary cache memory for processors with built-in cache and burst interfaces. Using SSRAMs in other applications can be tricky because of the timing assumptions built into the memory. The Pentium and PowerPC processors, for example, need two clock cycles to initiate a data transfer. The first clock sets up the address with data transfer occurring on the second clock in a burst transfer, the third and subsequent clocks also transfer data. The SSRAM, therefore, expects to have two clock cycles in which to begin memory transfer.

If your application doesn't use one of these processors and you need to perform a read-write-read sequence, there's a problem. Because it is expecting a burst with a known addressing sequence, the SSRAM has already begun a second memory cycle before the first cycle finishes. That partial cycle gets aborted when the SSRAM must suddenly turn its data direction around. This interruption forces use of a dummy cycle to clear the memory's data bus. The dummy cycle may occur either before or after a read cycle, depending on how you implement your control logic.

With careful design, you can avoid most of the problems presented by synchronous memories. On the positive side, synchronous memory interfaces simplify system timing by reducing the need to produce carefully controlled pulses. The interfaces also extend the effective speed of the memory. The main barriers holding synchronous memories back from widespread adoption are their price premium and the lack of standardization among vendors. Both concerns will be eliminated over the next two years. So, despite the problems currently associated with their use, synchronous memories represent the approach that high- performance systems will eventually have to adopt. EDN

Acknowledgment

I would like to thank American Microsystems Inc for sharing its expertise on designing ASICs with synchronous memory.

You can reach Technical Editor Rich Quinnell at (408) 685-8028; fax (408) 685-8028.

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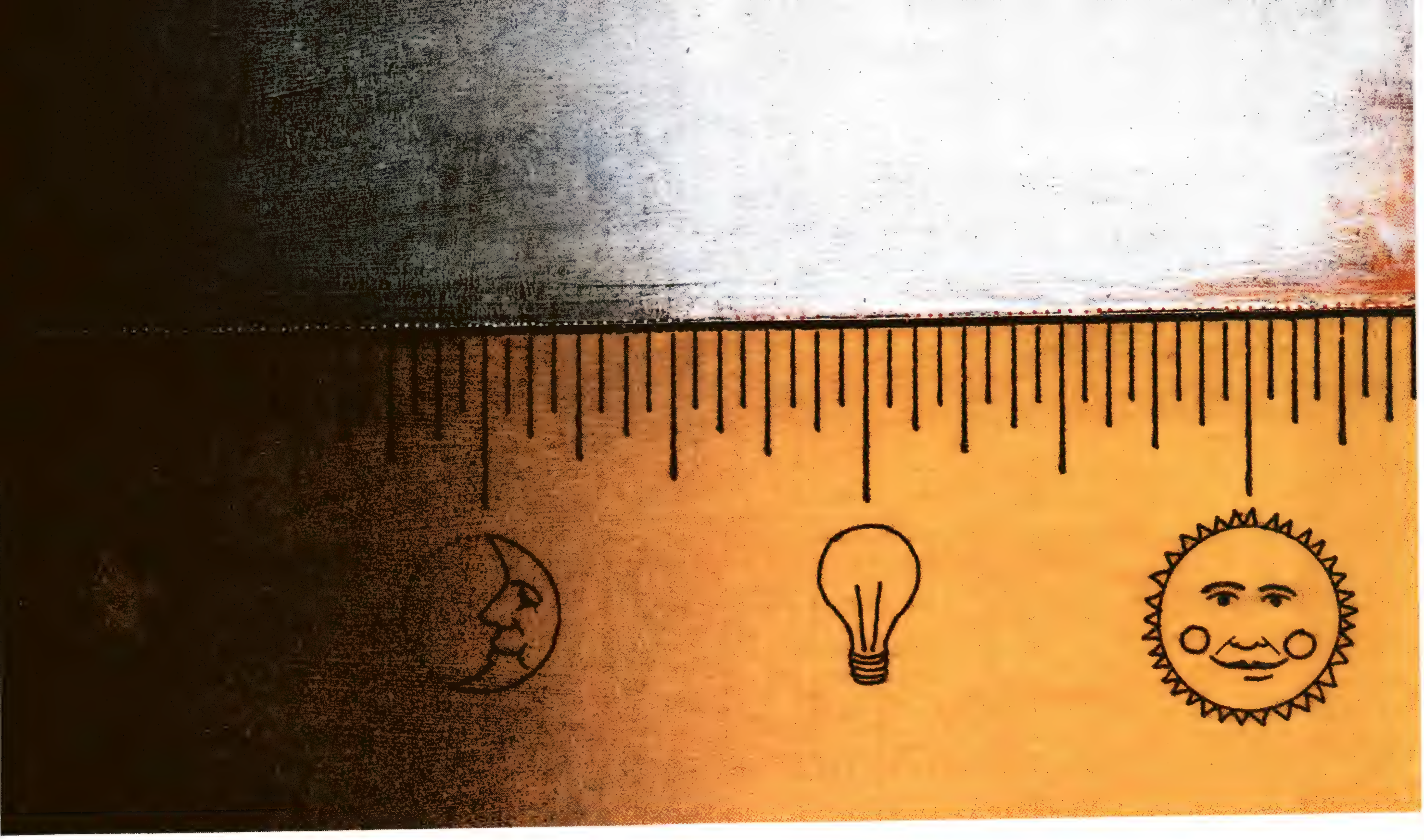

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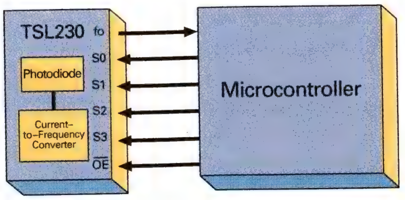

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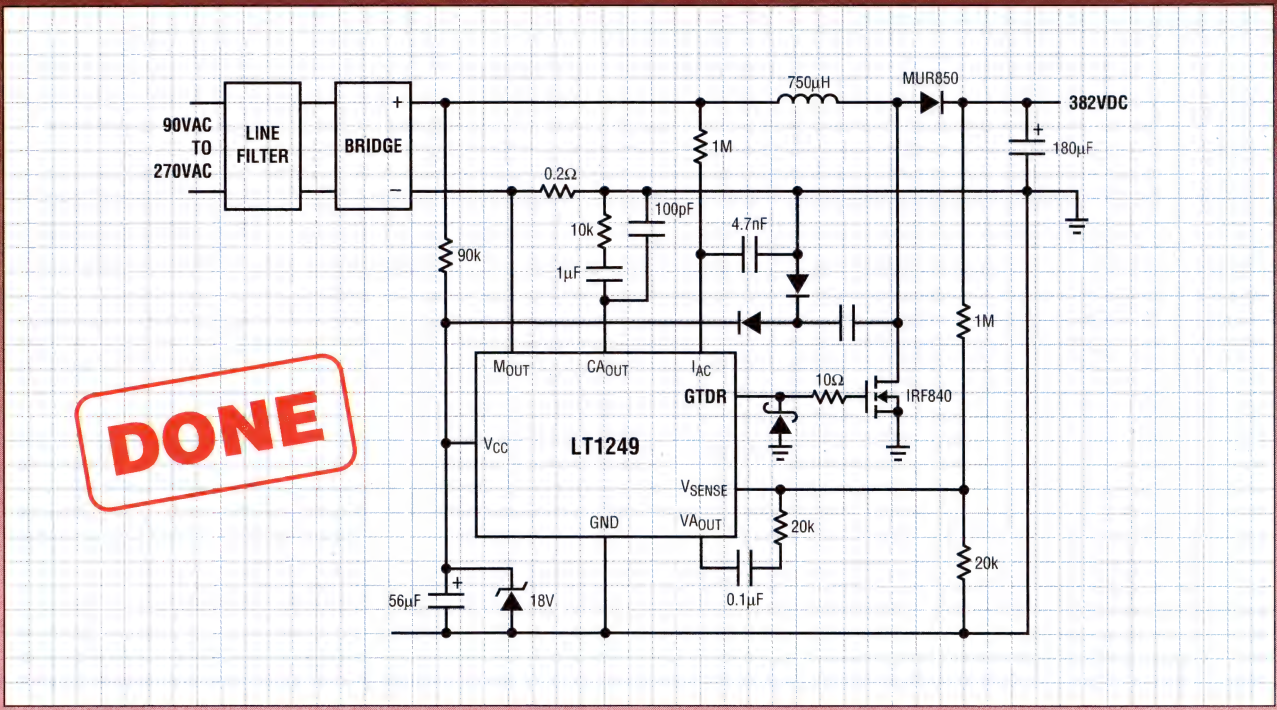

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CIRCLE NO. 148

RC network eliminates precision reference

Christophe Basso, European Synchrotron Radiation Facility, Grenoble, France

The circuit in **Fig 1** uses a magneto-resistive sensor to detect small magnet displacements without resorting to a precision voltage reference. A simple RC divider takes the place of the reference, eliminating an expensive component and obviating trimming each circuit.

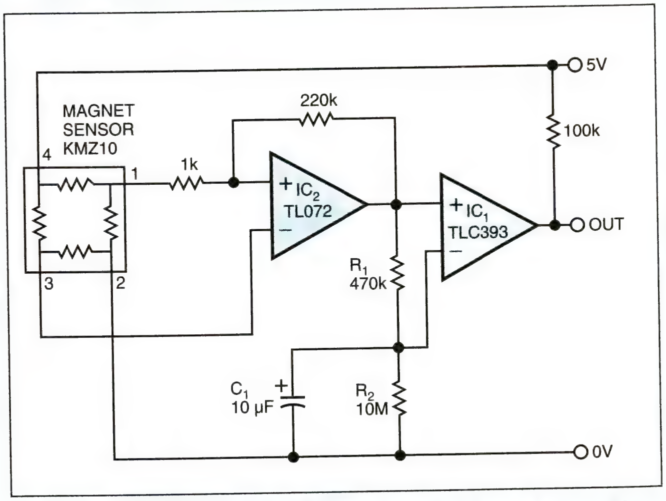


Fig 1—Minute changes in the magnet sensor's output cause IC_2 to develop a voltage across R_1. This configuration allows the circuit to detect small changes in sensor output without resorting to comparing the output to a precision voltage reference.

In the quiescent state, the resistive divider R_1/R_2 forces comparator IC_1 to be in a high state. Now, if the output of op-amp IC_2 starts to diminish, the voltage on the inverting input of IC_1 stays constant because of C_1. If IC_2's voltage variation is large enough to reverse the voltage across R_1 and reach the offset voltage of IC_1, IC_1's output switches to ground.

You can easily adjust IC_1's switching threshold by changing the value of R_1. The voltage difference across R_1 sets the circuit's sensitivity. The bigger R_1 is, the smaller the sensitivity.

Of course, the R_1-C_1 time constant sets the time the comparator takes to toggle back to its initial state. But, because of the high value of R_1 and R_2, you can achieve long time constants. The system simply needs more time to reach its final state after a power-on cycle.

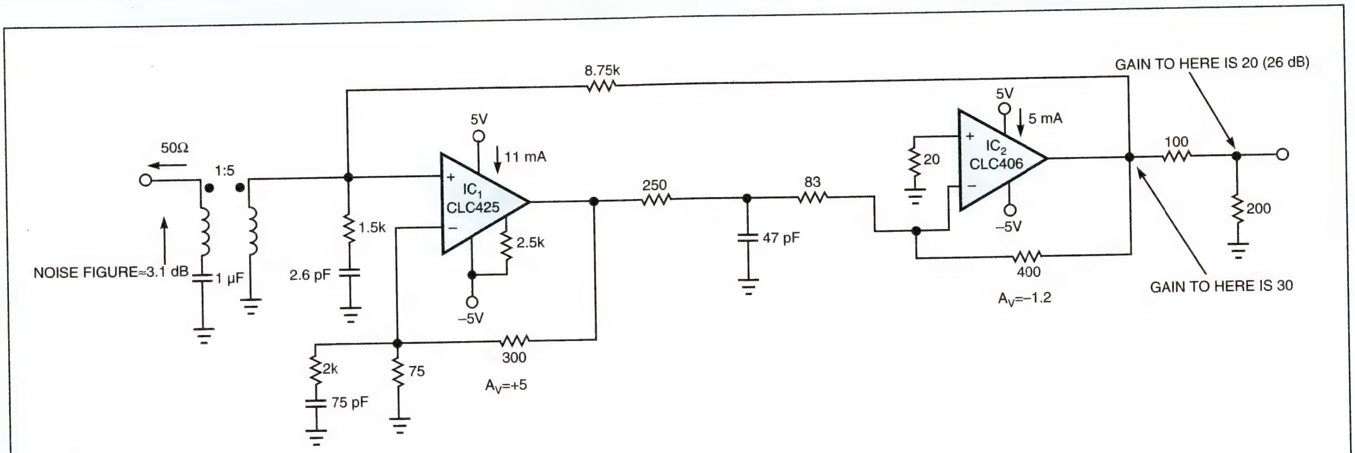
If you add another comparator wired as an OR to the first one, plus an RC circuit connected to the 5V supply, the circuit can also detect positive variations. (DI #1564) EDN

To Vote For This Design, Circle No. 320

Composite amplifier improves noise

Rea Schmid, Comlinear Corp, Fort Collins, CO

Amplifying low-signal levels for signal processing often stretches a single op amp's abilities. A composite design can improve the input noise for detecting extremely small signals and can enhance output-drive ability. Both the op amp's noise terms and the thermal noise of the components limit the minimum noise in an op-amp-based design. Furthermore, amplifier noise figures are not at their minimum for low-impedance sources such as 50Ω. Using a transformer is a common tech-



NOTES:
TRANSFORMER=T5-1T (0.3- TO 300-MHz RANGE), MINI-CIRCUITS, BROOKLYN, NY.
POWER-SUPPLY DECOUPLING NOT SHOWN.

Fig 1—This composite amplifier improves noise by 3 dB for detecting small signals.

nique to achieve matched input impedance for maximum power transfer. **Fig 1** shows one example, which follows the transformer with a composite amplifier to achieve a lower input noise figure.

Fig 1's composite circuit provides a method of setting the input impedance at the noninverting input by dividing the 8.75-kΩ feedback resistor by the forward gain plus 1. The circuit further divides this input impedance by the square of the turns ratio to match the source impedance.

The 1.5-kΩ resistor and 2.6-pF capacitor control the frequency response of the transformer without adding noise. For lower gain operation, the resistor/capacitor network in parallel with the 75Ω resistor provides compensation to stabilize IC_1. IC_2 inverts the signal and provides stability for the overall composite design. The 47-pF capacitor that splits the 250 and 83Ω gain-setting resistors adds a pole for noise reduction and stability. Since both op amps have wide bandwidths, the transformer limits the circuit's bandwidth. The measured noise of 3.1 dB is close to the calculated value of 3 dB and is a 3-dB improvement compared with using a single amplifier.

IC_1 was selected on the basis of it low-voltage and current-noise values of 1.05 nV/Hz and 1.6 pA/Hz, respectively. IC_2 was selected because it offers stable unity gain and a large full-signal-power bandwidth. Adding a 2.5-kΩ resistor to IC_1 lowers its quiescent current. (DI #1571)

To Vote For This Design, Circle No. 321

Isolation transformer passes millihertz signals

George Kassabian, University of California, San Diego, CA

You can successfully use an ordinary low-cost line transformer as an isolation transformer in ac circuits that require floating sources. However, at frequencies below 20 to 30 Hz, high distortion and excessive phase shifting occur. The simple circuit in **Fig 1** restores the phase and frequency response down into the millihertz region. Based on phase-response data, the low-end frequency response extends below 100 mHz.

The circuit samples the current at the end of the primary winding and applies frequency-dependent positive feedback. As the frequency goes below 50 to 60 Hz, the permeability of the iron core severely degrades, as does the inductance. This change causes a proportional increase in current at sense resistor R_S. The circuit ac couples this error voltage and injects it into the noninverting input of the op-amp driver.

The setting of R_S depends on the loop gain of the stage, losses in the primary winding, and the source load of the secondary. You can excite the circuit with a low-frequency triangular or square wave and adjust R_S for minimum distortion at the output. The transformer in **Fig 1** is wired in series to obtain high initial inductance, and a nonconcentric secondary provides for minimum capacitance between windings (approximately 25 pF). Isolation is rated to 2000V. Any op amp with fairly low 1/F noise, such as the LF356 or even lower noise OP-07, is suitable for this circuit. (DI #1577)

To Vote For This Design, Circle No. 322

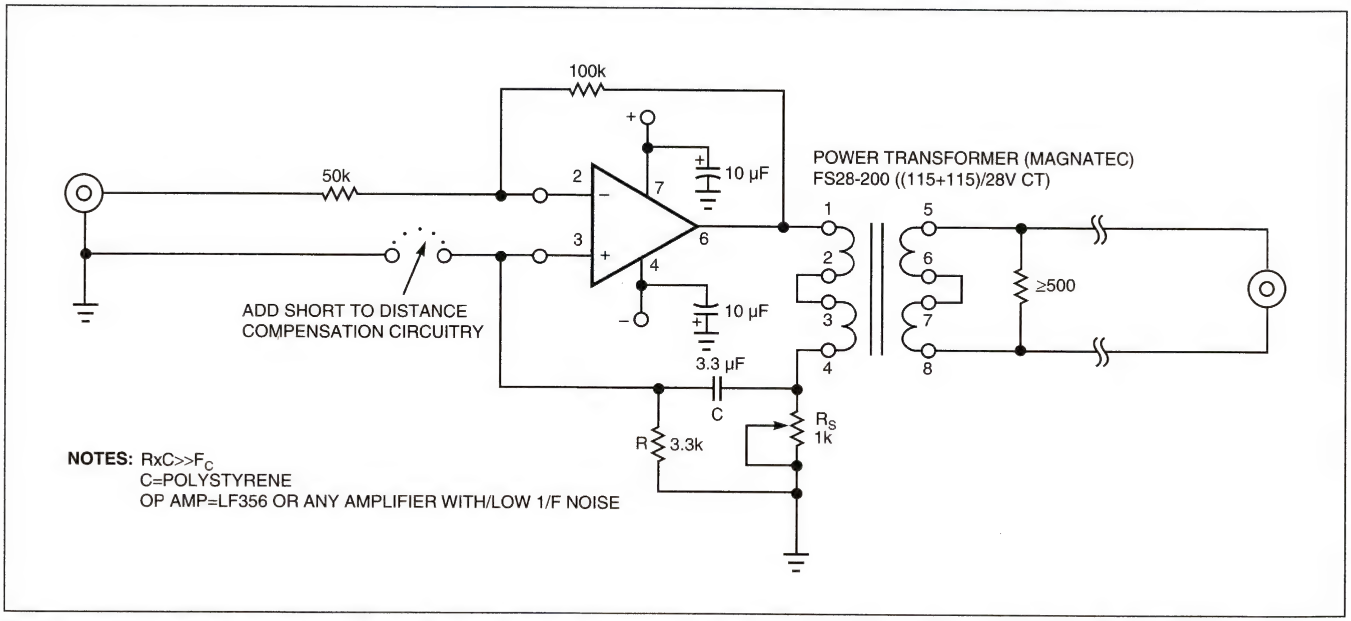


Fig 1—Positive feedback allows this circuit to extend an isolation transformer's frequency response down into the millihertz region.

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CIRCLE NO. 149

F 71 Rev F

Spice accepts and displays Y parameters

Michael A Wyatt, Honeywell SSAVD, Clearwater, FL

Admittance or **Y** parameters have been the favorite of many high-frequency analog engineers for many years. **Y** parameters provide insights into circuit behavior not as apparent as with the more popular **S** parameters. Although **S** parameters suit single-stage designs, modeling techniques that are impedance independent—namely **Y** parameters—suit IC designs best.

Standard Spice models don't accept **Y** parameters directly, and standard Spice cannot display complex functions such as **Y** parameters. You must generate special models or subcircuits to accept these **Y** parameters. Luckily, enhanced versions of Spice *can* display **Y** parameters directly.

Figs 1 and **2** illustrate methods to extract **Y** parameters from test-transistor Qtest. **Fig 1** pertains to $\mathbf{Y}_{11}$, $\mathbf{Y}_{21}$; **Fig 2** covers $\mathbf{Y}_{22}$, $\mathbf{Y}_{12}$. **Fig 1a** insinuates an image device, Qimage, which is identical to the test device, Qtest.

Qimage is embedded in a closed-loop current-control system comprising the set current-source Iset, current-controlled current-source F1, voltage-controlled current-source G1, and gain-resistor R1. This control system forces the collector current of Qimage to equal Iset. Voltage-controlled current-source G2, which is identical to G1, applies base current to Qtest while maintaining an ac-input open circuit.

Because G1 and G2 are identical and Qtest and Qimage are identical, Qtest's collector current equals Qimage's. Qimage's collector current is, in turn, equal to Iset.

The independent voltage-source Vce supplies collector-to-emitter bias voltage for both transistors while maintaining an ac-output short circuit. Qtest is outside the control system and input ac-current-stimulus Iinput has no effect on bias conditions.

Figs 1b and **1c** are plots of $\mathbf{Y}_{11}$ and $\mathbf{Y}_{21}$ vs frequency for Qtest. By definition, $\mathbf{Y}_{11}$=Iin/Vin and $\mathbf{Y}_{21}$=Iout/Vin. Therefore, plotting the real and imaginary portions of I(Iinput)/V(Iinput) and I(Vce)/V(Iinput), respectively, (with Voutput shorted to ground by Vce) gen-

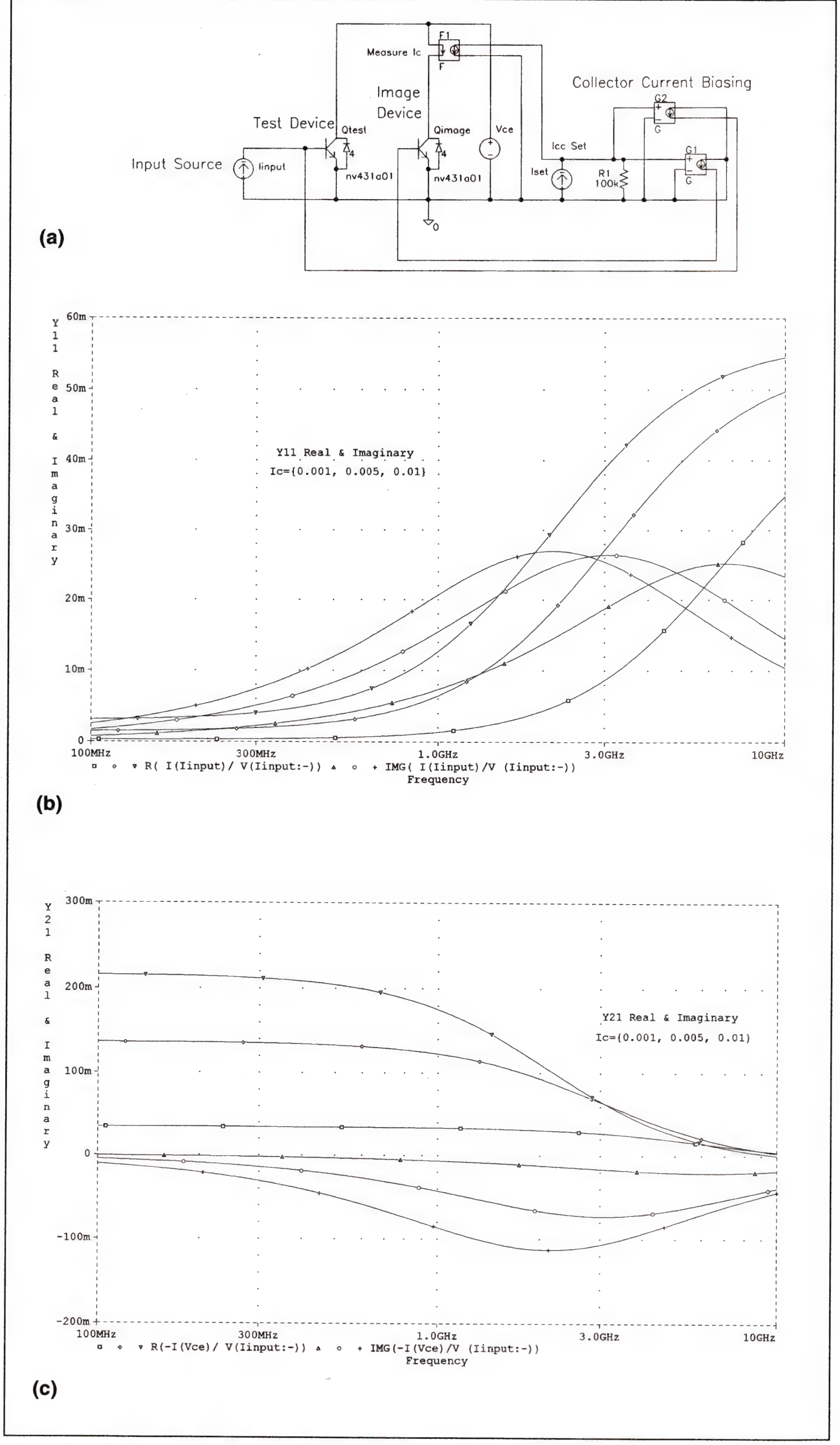

Fig 1—Adding an "image device," or twin of the device under test, to a Spice model (a) allows you to extract plots of Y_{11} (b) and Y_{21} (c) vs frequency.

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erates these graphs. (The parametric-analysis feature of pSpice, the enhanced Spice version I used, varied the collector current of Qtest from 1 to 5 mA.)

Extract $\mathbf{Y}_{22}$ and $\mathbf{Y}_{12}$ in a similar manner to that used for **Fig 1a**. Except in **Fig 2a**, voltage-controlled voltage-sources E1 and E2 replace voltage-controlled current-sources G1 and G2. And an ac-output voltage-stimulus Vout replaces the ac-input current-stimulus Iinput. E1 maintains an ac short circuit on the input to Qtest, while Vout stimulates Qtest's output. Again, given that $\mathbf{Y}_{22}$=Iout/Out and $\mathbf{Y}_{12}$=Iin/Out, plotting the real and imaginary portions of –I(Out)/V(Out) and –I(E1)/V(Out) generates, respectively, the graphs in **Figs 2b** and **c**.

You can use an enhanced Spice package's parametric-analysis capability to plot the **Y** parameters as functions of collector/emitter voltage, temperature, or other parameters. (DI #1563) EDN

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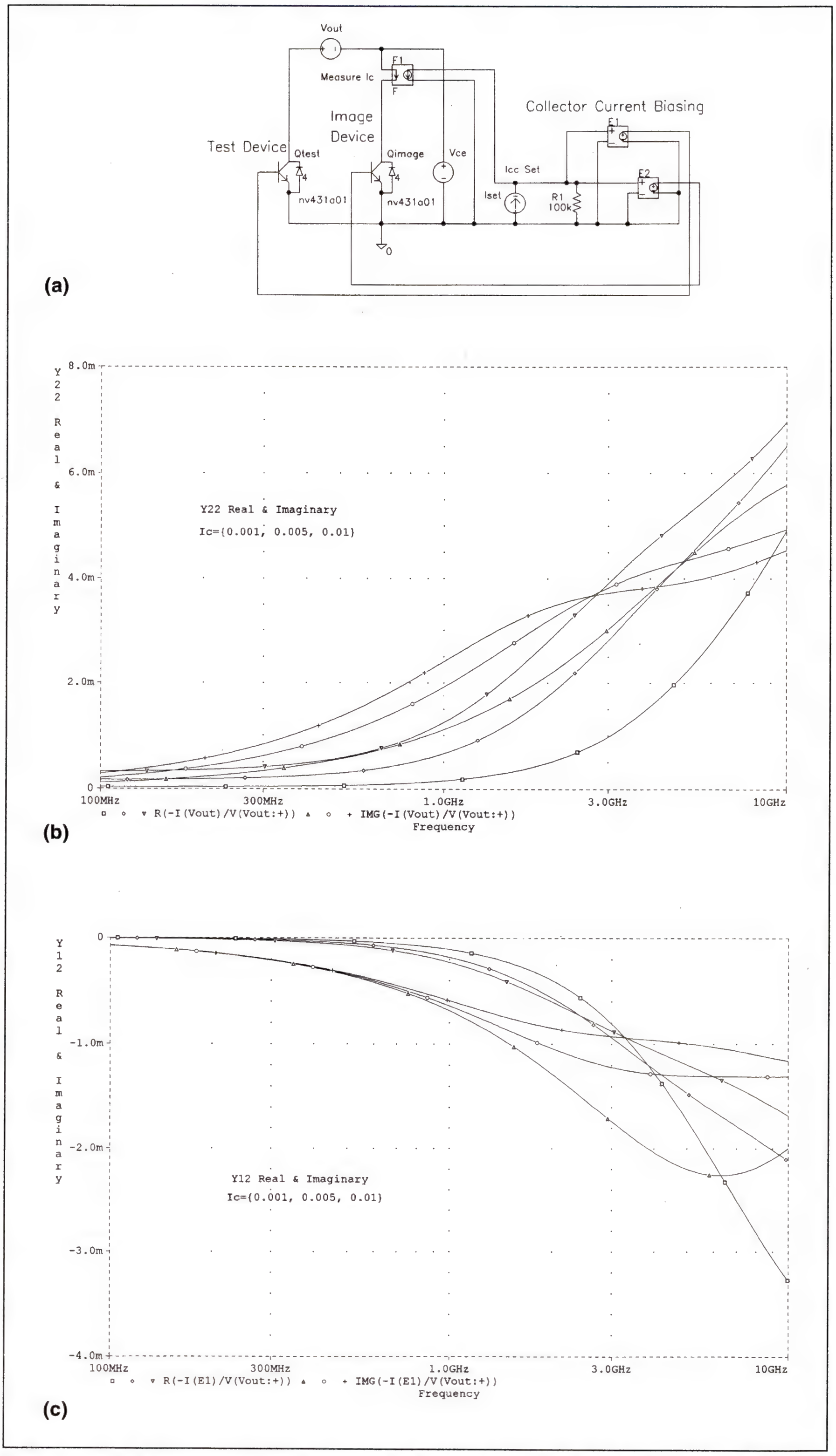

Fig 2—Using the same technique as in Fig 1, the Spice program in (a) rounds out your set of Y parameters, yielding Y_{22} (b) and Y_{12} (c).

LINEAR TECHNOLOGY DESIGN NOTES

Interfacing to Apple LocalTalk® Networks

Design Note 85

Robert Reay

LocalTalk Overview

Of the many connection technologies available for linking an AppleTalk® network, LocalTalk is one of the most common because it is designed to connect local work groups using inexpensive and easily configurable plug-and-play cabling. LocalTalk is laid out in a bus topology with all devices joined in a line with no circular connections. LocalTalk conforms to the EIA RS422 electrical standard to provide a balanced differential voltage signal transmitting at 230.4kbs over a maximum distance of 300 meters with up to 32 devices connected to a twisted-pair network. The balanced configuration provides good isolation from ground noise currents and is not susceptible to fluctuating potentials between system grounds or common-mode electromagnetic interference (EMI).

LTC1323

The original LocalTalk hardware design uses an AM26LS32 chip for the receivers and an AM26LS30 chip for the drivers of a LocalTalk port. The drawback of the design is that it requires two chips per port and an external –5V supply. The bipolar chips also draw large supply currents, making them undesirable for battery-powered applications. A better solution is to use the LTC1323CS24 which provides a complete low power serial I/O interface while generating it's own –5V supply as shown in Figure 1.

The LTC1323 uses the differential driver output stage of Figure 2. The driver swings between ground and V_{CC} when a differential LocalTalk load is connected between TXD^+ and TXD^- while meeting the EIA RS422 differential voltage swing requirement of ±2.0V into 100Ω. When a single-ended load is connected from TXD^+ to ground or TXD^- to ground, the driver will swing between V_{EE} and V_{CC} while meeting the EIA 562 voltage swing requirement of ±3.7V into 3kΩ. Because the differential LocalTalk load requires a large current drive, the charge pump that generates V_{EE} would be unreasonably large if the driver were to swing to V_{EE} with a differential load. By limiting the current flowing into V_{EE} to 15mA, the charge pump can easily be integrated into the chip.

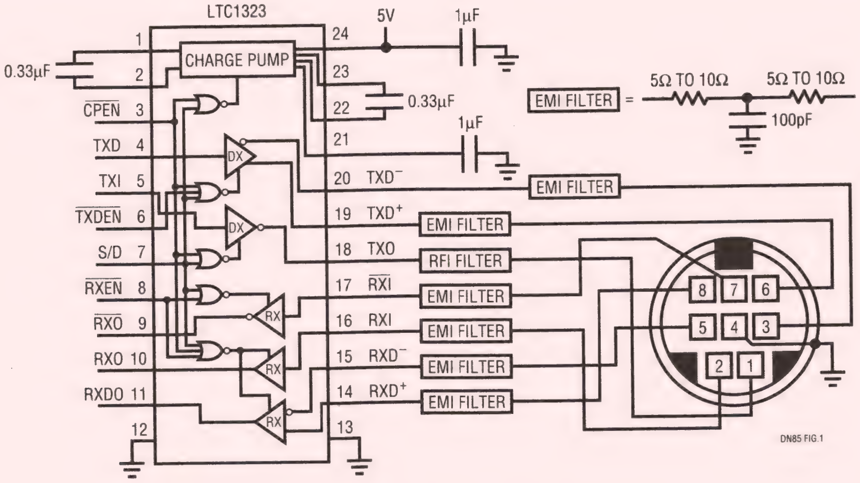

Figure 1. Single Supply LocalTalk Port

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For applications where the single-ended control signals are not required, such as PhoneNet®, the LTC1323CS16 can be used as shown in Figure 3. The differential driver is still able to drive a single-ended load to V_{EE} when not connected to a LocalTalk network.

LTC491

For PhoneNet-type applications where the differential driver is not required to drive a single-ended load below ground, the LTC491 can be used as shown in Figure 4. Only RS485 drivers will work in this application. RS422 drivers will not work because they load the cable when the chip power is removed.

EMI Filter

Most LocalTalk applications use an electromagnetic interference (EMI) filter consisting of a resistor-capacitor T network between each driver and receiver and the connector (Figure 5). Unfortunately, the resistors significantly attenuate the driver's signal applied to the cable. Because the LTC1323 and LTC491 are single supply drivers, the resistor values should be reduced to 5Ω to 10Ω to insure enough voltage swing on the cable. In most applications, removing the resistors completely does not cause an increase in EMI as long as a shielded connector and cable are used. With the resistors removed, the only DC load becomes the primary of the LocalTalk transformer. This will increase the DC standby current when the drivers are active, but does not adversely affect the drivers because they can handle a direct short circuit indefinitely. For maximum swing and EMI immunity, a ferrite bead and capacitor could be used.

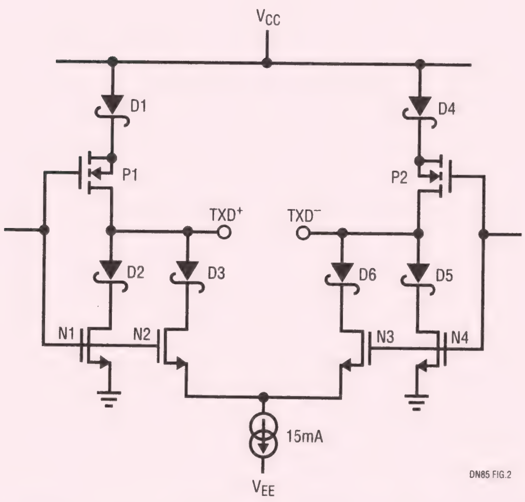

Figure 2. LTC1323 Differential Drive Output Stage

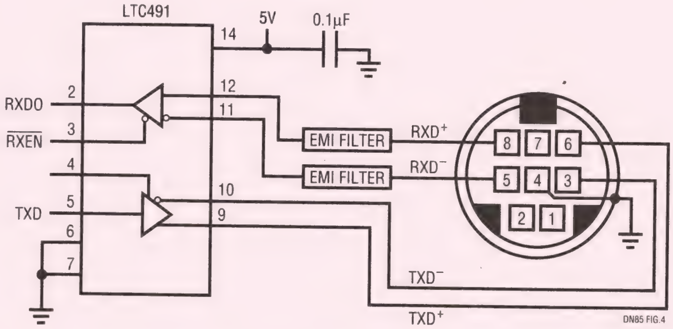

Figure 4. PhoneNet Application

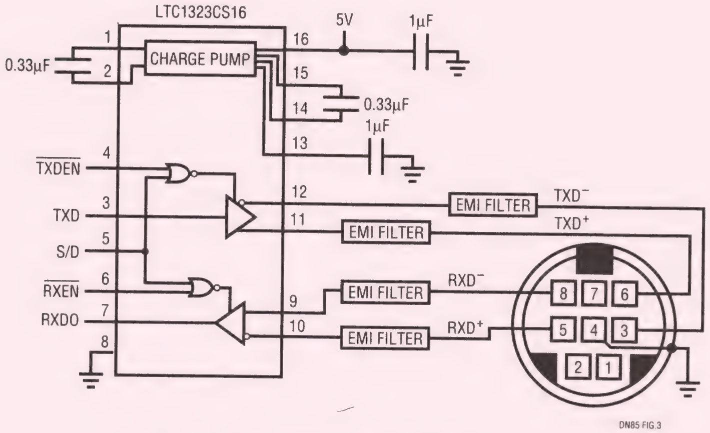

Figure 3. PhoneNet Application

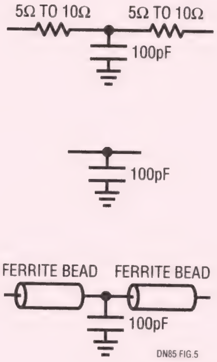

Figure 5. EMI Filters

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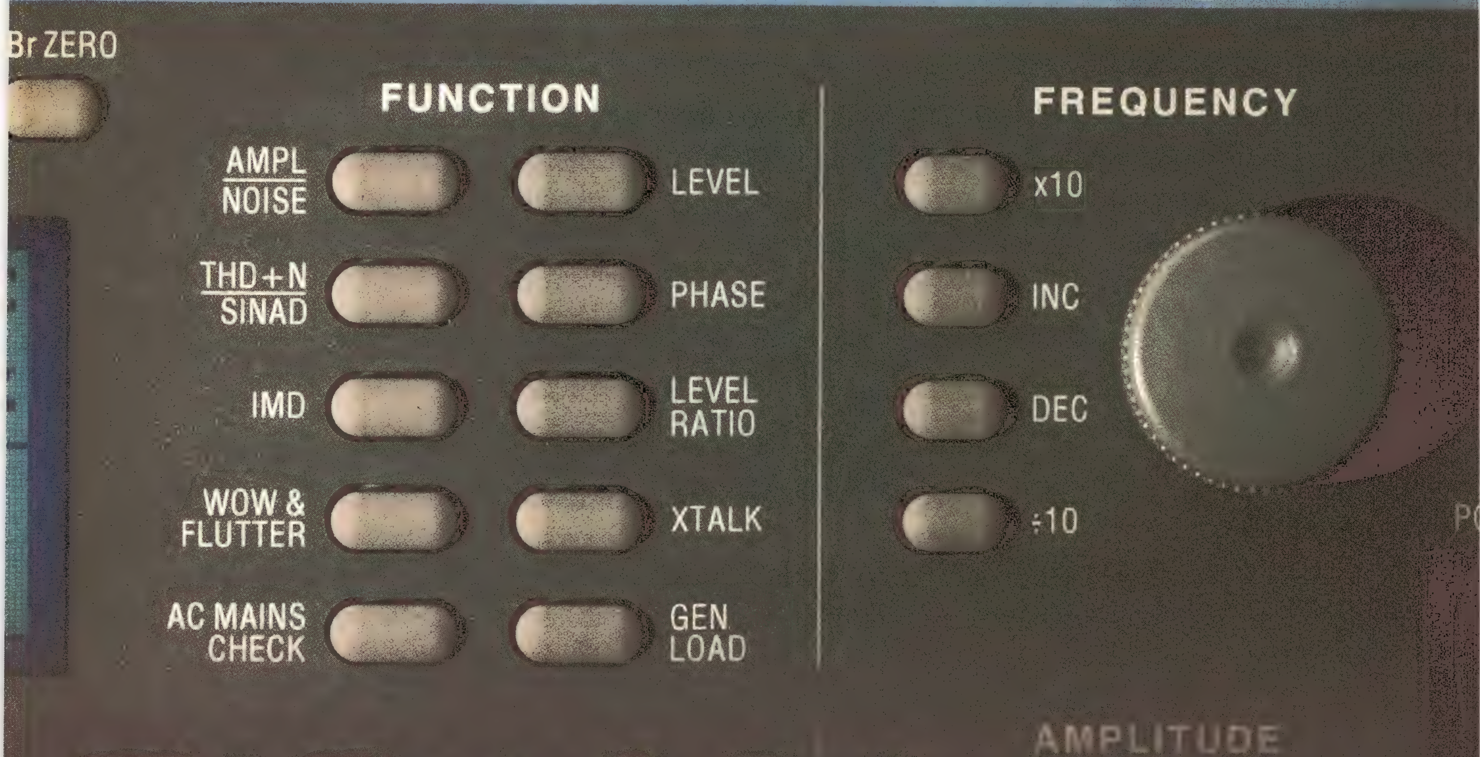

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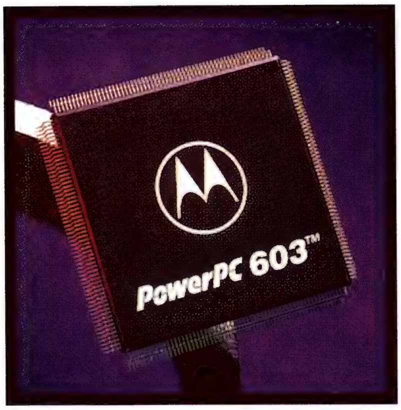
CIRCLE NO 71



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CIRCLE NO. 83

Noise-figure curves ease the selection of low-noise op amps

John W Christensen, National Semiconductor Corp

Evaluating plots of noise figure vs source resistance makes it easy to select a low-noise amplifier for a given source resistance. A BASIC program calculates the numbers from data-sheet parameters.

Selecting the right op amp can be a serious challenge when you take all of the possible parameters into consideration. Choosing a low- noise amplifier is particularly daunting. Both internal and external sources of noise, including many that designers ignore or don't recognize, affect the op amp's and overall system's noise performance. Different types of op amps—CMOS, JFET, and bipolar—exhibit various noise characteristics about which you can make some dangerous generalizations. However, an important tool, namely using low noise figure (NF) for given source resistance, does exist to help take some of the guesswork out of choosing a low-noise amplifier.

Unfortunately, many designers aren't even aware that they need such a tool, and they think all the information they need is on the data sheet. They usually just look at the voltage noise (e_n) numbers on the data sheet and use the "if it's lower, it's better" method. The problem with this method is that it ignores the current-noise (i_n) half of the equation (see **box**, "Internal and external op-amp noise sources." By ignoring the effects of current noise, you ignore the effect of the source resistance on the amplifier's noise performance. The total noise voltage, e_{nt}, at the input of an amplifier is

$$e_{nt} = \sqrt{e_n^2 + (i_n \cdot R_S)^2}. \qquad \textbf{(1)}$$

This number is absolutely necessary for determining the noise performance of a system. Just looking at e_n alone can be very misleading. For example, compare the performance of two popular op amps, the LMC662 and the OP-07, when amplifying a signal from two source resistances. At first, the OP-07 with a typical 1-kHz noise voltage of 9.6 nV/√Hz would appear an easy winner over the LMC662 with a typical 1-kHz noise voltage of 22 nV/√Hz. But when you look at the noise currents, you find the opposite is true: 120 fA/√Hz for the OP-07 vs 0.113 fA/√Hz for the LMC662.

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To illustrate the effects of these differences, compare signals coming from a 10-kΩ and a 10-MΩ source. Determining the noise contribution of the amplifier requires only an rms addition of the effects of the noise current and noise voltage. In the case of the OP-07, using **Eq 1**,

$$e_{nt} = \sqrt{(9.6\ \text{nV}/\sqrt{\text{Hz}})^2 + (120\ \text{fA}/\sqrt{\text{Hz}} \cdot 10\ \text{K}\Omega)^2} = 9.67\ \text{nV}/\sqrt{\text{Hz}}. \qquad \textbf{(2)}$$

As you can see, the OP-07 noise current makes no real difference at this source resistance. The much lower noise cur-

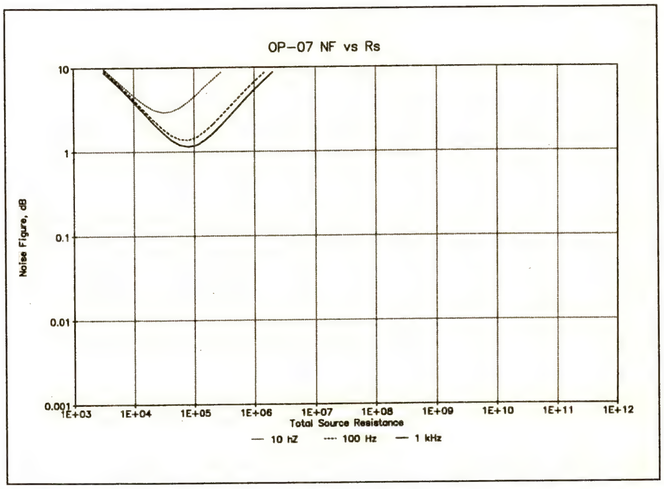

Fig 1—These NF-vs-source resistance curves show that the OP-07 exhibits its optimal noise performance when the source resistance is in the range of 10 kΩ to 1 MΩ.

rent of the LMC662 has even less effect, so the 22 nV/√Hz is the total noise contribution. In this case, the OP-07 is the easy low-noise winner.

If you perform the same calculations for the OP-07 with a 10-MΩ, the result is

$$e_{nt}^2 = \sqrt{(9.6\ \text{nV}/\sqrt{\text{Hz}})^2 + (120\ \text{fA}/\sqrt{\text{Hz}} \cdot 10\ \text{M}\Omega)^2} = 1200\ \text{nV}/\sqrt{\text{Hz}}. \quad \textbf{(3)}$$

At this source resistance, the e_{nt} of 1200 nV/Hz makes the "quiet" OP-07 a very noisy choice. However, for the LMC662,

$$e_{nt} = \sqrt{(22\ \text{nV}/\sqrt{\text{Hz}})^2 + (0.2\ \text{fA}/\sqrt{\text{Hz}} \cdot 10\ \text{M}\Omega)^2} = 22\ \text{nV}/\sqrt{\text{Hz}}. \quad \textbf{(4)}$$

In this case, the OP-07's total noise voltage is 55 times higher than the LMC662, making the LMC662 the low-noise choice. From these extreme examples, it is obvious that selecting a low-noise op amp requires more than just looking at e_n.

Justifying the use of NF

NF is a convenient way to describe the ratio between the total system noise and the theoretical source-resistance noise. An RMS addition of the noise contributed by the amplifier with that of the source results in the noise present at the input of the amplifier. Twenty times the log of the ratio of this sum to just the noise from the signal source equals the NF.

$$\text{NF} = 20\log_{10}\left(\frac{\text{SYSTEM S/N RATIO}}{\text{SOURCE S/N RATIO}}\right). \quad \textbf{(5)}$$

NF is a common parameter for comparing RF amplifiers or ac circuits, which allows you to transform the signal resistance to match the amplifier. Over the years, op-amp experts have implied that because you can't adjust the source resistance of a dc circuit (adding resistance to a source because it is lower than optimum only results in more noise and less signal), then knowing the NF at other resistances is useless information.

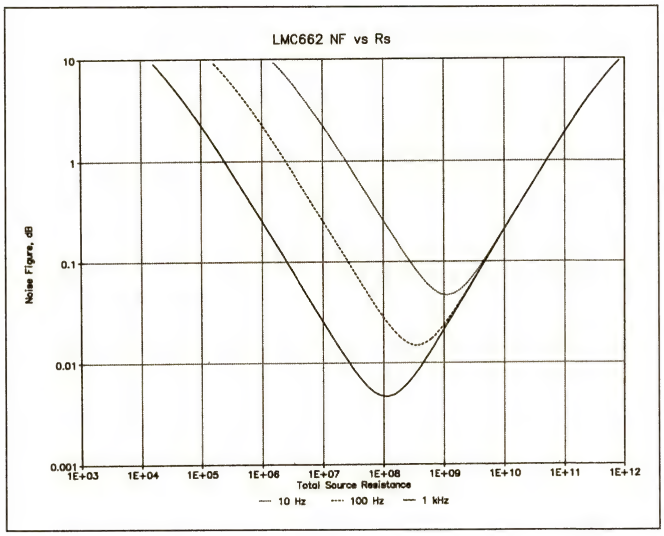

Fig 2—At source resistances from 100 kΩ to 10^{11}Ω, the LMC662 is a good low-noise choice.

This viewpoint may have been true when there wasn't such a wide variety of op-amp choices, but the situation is quite different today. Because several op amps may meet the basic requirements of bandwidth, slew rate, and drift, selecting the one with the lowest for the existing source resistance *is* practical.

Another argument against using NF is based on the premise that, because any source resistance causes the noise current to add to the noise voltage, the lowest system noise is obtained when the source resistance is zero. Calculating the NF for a system with zero source resistance always gives an infinitely high NF (the denominator of **Eq 5** is zero). Therefore, if the source resistance is zero, selecting for lowest NF does not give the lowest system noise.

These statements are also true but irrelevant. In the real world, zero source resistance would require infinite signal power, and if you had infinite signal power, you wouldn't need an amplifier.

Note that there is also the case of the purely reactive source. A signal from a lossless capacitor or inductor has no thermal noise, and the selection process would be quite different from that of resistive sources. For more discussion on reactive sources, see **Ref 1**.

Calculating NF

Although almost no op-amp manufacturer provides NF curves, most data sheets do include the information (namely, e_n and i_n) necessary to plot these curves. Using these voltage- and current-noise numbers and performing a few calculations, you can determine the NF for any amplifier at the resistance of interest. To make the process even easier, a Basic program automatically calculates NF over a wide range of resistance values and generates an ASCII file of NF numbers (see *EDN*'s computer bulletin-board system (BBS).

Figs 1 and **2** show the plotted NF results using data from the OP-07 and LMC662 data sheets. The log dB scale of the NF graphs shows how close to zero the NF will go but still provides detail at the higher noise levels. To make comparisons easier, the horizontal and vertical scales of all the plots are identical. The curves owe their shape to the large contri-

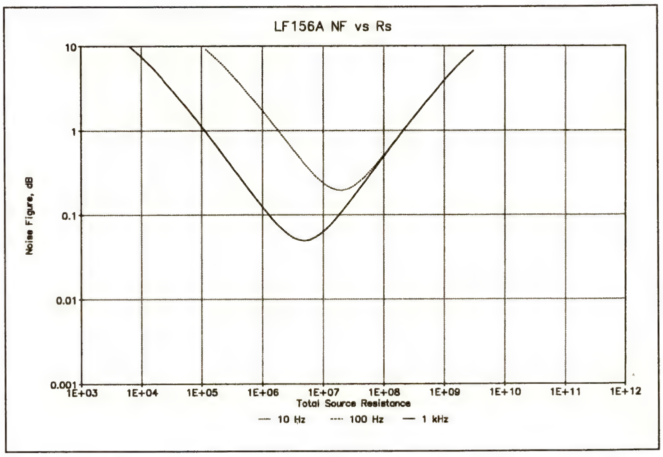

Fig 3— The LF156A is an example of a low-noise amplifier for sources of 20 kΩ to 1 GΩ.

bution of amplifier-noise voltage on the left and descending side and to the noise-current contribution, which causes the NF to begin rising to the right.

The curves clearly point out that at 10 kΩ, the NF for the OP-07 is 4 dB. At this source resistance, the LMC662 has an NF of 11 dB, making the OP-07 the easy winner. How-

INTERNAL AND EXTERNAL OP-AMP NOISE SOURCES

The easiest way to represent the noise parameters of an op amp is to assume there are two separate, uncorrelated noise generators at the inputs of an ideal noiseless op amp: a noise voltage source in series with an input and a noise-current generator connected between each of the inputs of the amplifier and ground (**Fig A**).

The value of the source resistance has no effect on the internal noise-voltage source because the source resistance is in series with the input. However, because the current-noise sources are between the two inputs and ground, the contribution due to these sources is directly related to the source resistance.

This noise current flows through the source and anything else connected to the inputs, such as the feedback resistance. This current produces a noise voltage proportional to the total impedance seen from the inputs. As a result, this contribution depends upon the value of the source resistance. These two noises add at the amplifier input and appear as the amplifier's contribution to the total system noise (**Eq 1**).

Recognize other noise sources

Noise can corrupt a signal in more ways than through these voltage- and current-noise sources, and many contributors to noise go unrecognized. For example, air currents flowing over a pc board generate low-frequency signals. These air currents produce small fluctuations in temperature at the thermocouple junctions produced where the IC is soldered into the board. Most system designers are not aware that the common IC lead frame material, Kovar, and the copper board traces produce effective thermocouples, which produce about 35 μV/°C.

A low-noise bipolar op amp, such as the OP-07, has a typical 0.1- to 10-Hz noise of 0.35 μV p-p. If the lead frame were made of Kovar, the soldered connection on the board would need to wander around only 0.01° to produce a "noise" signal equal to that of the op amp. Because of the thermal mass of the board, this noise appears as 1/f noise starting below 2 or 3 Hz. This air-current "zephyr" noise may in fact be the 1/f noise shown on many low-noise op-amp data sheets.

There are two ways to eliminate this noise source. One is to prevent temperature fluctuations from occurring at all connections between the low-level signal source and amplifier's input by embedding a portion of the circuit in foam or enclosing it in a small, separate, closed box. Using amplifiers built on copper-lead frames, such as the OP-07, also eliminates this source of noise. However, internal connections of silicon and other metals, such as gold or aluminum, create thermocouples with outputs as much as 10 times higher than those produced by Kovar-copper connections. Thus, even copper lead frames are not a complete answer. Reducing thermal gradients is still necessary for the lowest system noise.

Excessive bandwidth is another source of noise that op-amp users often overlook. The bandwidth itself doesn't cause extra noise. However, most of the types of noise generated in the amplifier or inherent in the signal source are broadband generators, which the op amp then amplifies over its full bandwidth.

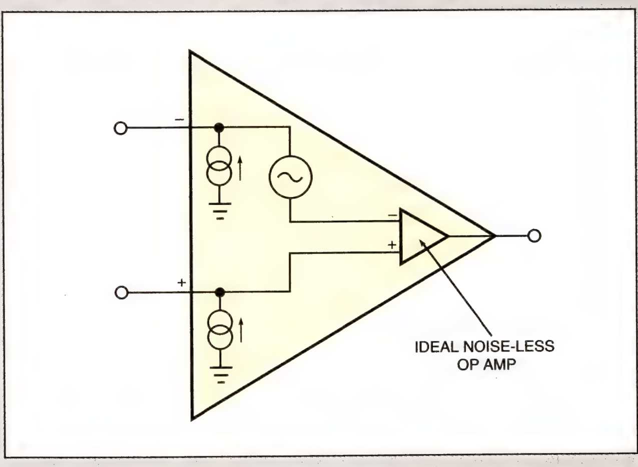

Fig A—The noise model of an op amp includes two separate, uncorrelated noise generators at the inputs to an ideal, noiseless op amp: a noise voltage source in series with an input and noise current generators between each input and ground.

Many signals do not require extremely wide bandwidths. To pass a 1-kHz square wave and maintain sharp edges requires an amplifier with a 10- to 20-kHz bandwidth. If the objective is to restore this signal when its amplitude is as small as the amplifier noise, you must first limit the maximum bandwidth of the incoming signal and the amplifier to around 1 to 3 kHz. This limit reduces the amount of noise being amplified with the signal. Limiting the low-frequency response of the system with a bandpass filter reduces the noise even further.

In addition to the voltage and current noise of the op amp itself, one other fixed noise source, external to the op amp, is significant: the signal source. Designers tend to assume that a signal source is noiseless, but, in reality, all resistive sources generate thermal noise proportional to the square root of the source's resistance. Using the formula

$$e_n = \sqrt{4\ KT \cdot BW \cdot R_s},$$

where K is Boltzman's constant (1.38×10^{-23} joules/kelvin), T is the temperature in kelvin, BW is the bandwidth in hertz, and R_s is the source resistance, you can calculate this noise voltage.

For example, at 25°C (298K) a 1-kΩ source produces a minimum noise of 4 nV/√Hz. This noise is always present, along with the signal, and determines the optimum SN ratio of the signal source.

ever, at 10 MΩ, the situation is reversed. The OP-07 now has an NF of 19.08 dB, compared with 0.025 dB for the LMC662. Thus, at 10 MΩ, the LMC662 is the low-noise winner.

The curve in **Fig 3** shows that the LF156A is a good example of an amplifier suitable for high source impedances. **Fig 4** shows that the OP-27 exhibits its lowest noise performance with low-resistance sources.

Even if a data sheet doesn't provide the i_n numbers, in some cases, you can still arrive at an approximate NF, which is theoretically the best NF. Specifically, if the input stage of the op amp doesn't use bias-current cancellation, you can use the input bias current to estimate a best possible case. To calculate the lowest possible noise current, you can use the formula for shot noise (noise that results from current flowing across a pn junction), which is

$$i_n = \sqrt{2 \cdot Q \cdot I_b \cdot BW}, \qquad \textbf{(6)}$$

where Q is the electron charge (1.6×10–19), BW is the bandwidth, and I_b is the bias current in amps. Don't forget that the input current of JFET op amps doubles for each 10°C increase in junction temperature. Thus, the resulting noise current increases by √2 with each 10°C rise. A conservative approach is to use the input current specified on the data sheet at the highest temperature.

If you question the usefulness of this number, you should know that the data sheet's i_n number for most CMOS and some JFET amplifiers is the result of this very calculation. The calculated 113 aA (10^{-18} amps) (700 electrons/sec rms)/√Hz for the LMC662 is much too small to measure in the real world. This noise current reduces the S/N ratio of a 1000-MΩ source by only 0.024 dB.

These calculated numbers are most useful when the source resistance is less than 1 GΩ. At higher source resistances, the number becomes more theoretical than practical. At the level of 113 aA/√Hz, the current has no real effect in almost all cases. For noise currents to have a meaningful effect, you must consider the true value of the source resistance. Resistors with values of 10^{12} Ω or more are available, but just 1 pF of shunt capacitance reduces the impedance at 100 Hz by a factor of over 600. For this reason, noise currents, such as those of the LMC660 family, normally have no effect. At high resistances, the noise voltage of the source is so much higher than the op amp that the resulting NF is nearly zero.

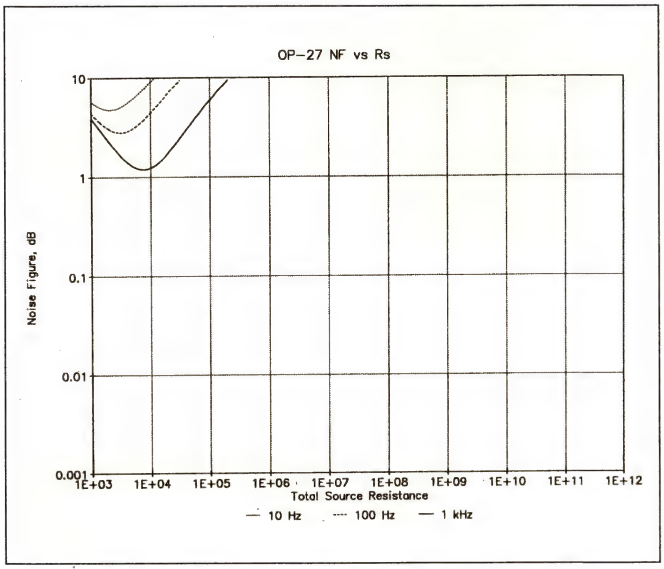

Fig 4—The OP-27 exhibits its lowest noise performance with low-resistance sources.

As you can see from the figures, the e_n of many op amps is not the limiting factor of low-noise performance. However, by selecting an amplifier with a low NF for the source resistance, you can design a low-noise system. An NF of 1 dB or less provides nearly ideal noise performance.

BiFET and CMOS op amps usually have higher noise voltages than do op amps with bipolar input stages. Contrary to popular opinion, using CMOS op amps with high-resistance signal sources can result in a low system NF. At lower source resistances, many bipolar op amps can provide good low-noise performance because of their low e_n. A quick look at the NF graphs can simplify selection.

Finally, remember that for many applications, the noise contributed by the amplifier may be insignificant compared with that of other parts of the system. Many of today's low-noise amplifiers have much lower noise than do most signal sources. Also, if the NF curves you generate show only minor differences between amplifiers—a 0.2-dB difference, for example—other, possibly more important, parameters such as power consumption, bandwidth, offset voltage drift, and price, may make more of a difference in your op-amp choice. EDN

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Author's biography

John W Christensen is a principal applications engineer at National Semiconductor and has been with the company for over 6 years. His hobbies include sailing and scuba diving.

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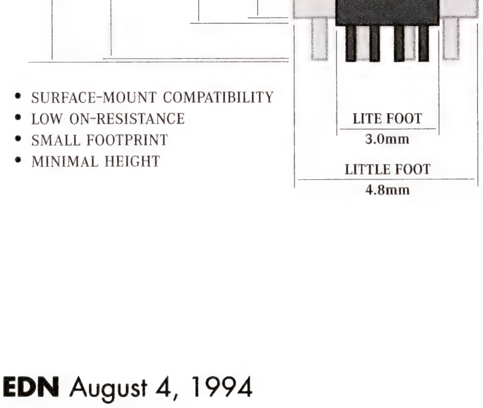

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Si6542DQ	Complementary			
	N-Ch	20	100	2.5
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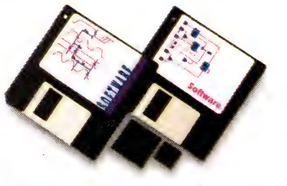

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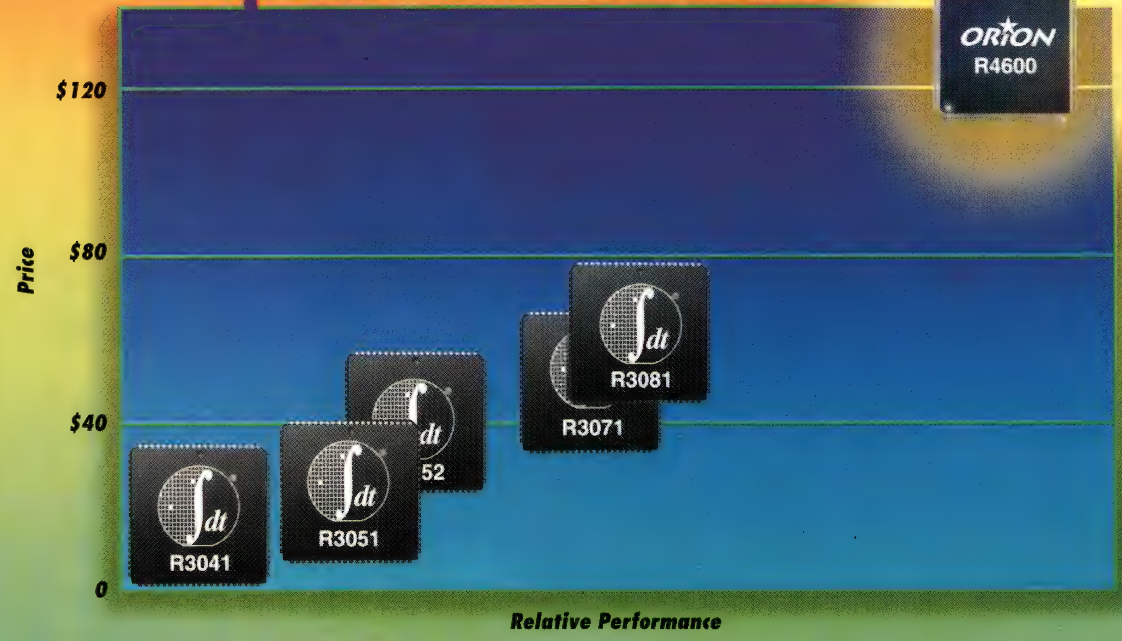

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Canny choices condense CPLD and FPGA design cycles

Sung C Hu, San Francisco State University

The proliferation of CPLDs and FPGAs has resulted in flexible devices that reduce design time and contribute to a design's smaller size, higher reliability, lower cost, and lower power consumption. However, you must choose from among many devices, each having its own diverse architecture.

Knowing which FPGA (field-programmable gate array) or CPLD (complex programmable-logic device) will match your application can save you significant design time. The first issue to resolve—but one which is beyond the scope of this article—concerns in-system versus off-line programmability. Next, you should determine whether a device's capacity and performance fit your application. Some simple selection guides in this article can help you compare various devices' capacity and performance. Once you resolve the fitness question, you can choose among a manageable number of devices, looking at cost, support, availability, etc (see **box**, "Articles that cover other aspects of multifaceted devices").

You can easily use all selection guides in this article without spending an enormous amount of time studying device architectures and performing abstruse fitting calculations. Because design involves a delicate balancing act where intuition plays a crucial role, no off-the-shelf benchmarks can replace experience.

Unfortunately, some of the most common metrics for FPGAs and CPLDs are worthless. Take, for example, a number borrowed from the gate-array world, the so-called equivalent-gate count. The count is the number of 2-input NAND gates needed to implement a given design that can also be implemented in the device. Because fundamental building blocks in most programmable devices are not NAND gates, gate-counting depends on the circuit selected for implementing and the vendor doing the counting. Besides, actual circuits seldom consist solely of 2-input NAND gates. Thus, gate count is not a good capacity measure for programmable devices. Other comparison parameters are the number of I/Os, macrocells, flip-flops, clocks, and speed or frequency.

Specifications not standardized

The lack of standardized specifications presents a major difficulty in interpreting vendor data books. In addition, data-book specifications are not necessarily usable. Take f_{MAX} as an example: this vendor specification often does not account for setup and hold times for register-to-register operations. Also, data books sometimes cite f_{MAX} without indicating whether the frequency is internal or external.

In addition, most devices' parameters change with operating conditions such as frequency, temperature, loading, voltage level, etc. But the industry has no standardized environment for measuring parameters.

Finally, vendors derive most of the their specifications from devices programmed with elementary logic structures that have little or no relation to real designs.

Interpreting PREP benchmark results

PREP benchmarks (**Table 1**), on the other hand, provide data derived from standardized tests in a standard format. Unfortunately, no recognized way of using PREP results exists, and every company will put its own twist on interpreting PREP benchmark results. Already some companies emphasize cost per instantiation while others stress the importance of system characteristics that are not benchmarked. Still other companies use biased "averages" of benchmark results, and accusations of misrepresentation and "unfair benchmarking" also exist. When reading advertisements, remember what Mark Twain once said, "There are three kinds of lies: lies, damned lies, and statistics."

Capacity comparison

One way to compare the capacities of different devices is to get the mean of the benchmark-repetition numbers for each device. Because benchmark circuits are of varying sizes, the simple arithmetic mean is *not* appropriate. For example, suppose that the repetition number of devices A and B for benchmarks 1, 2, and 3 are:

TABLE 1—ERRONEOUS AVERAGE CAPACITY

Benchmark	Device A	Device B
1	2	3
2	2	4
3	20	17
Arithmetic mean	8	8
Harmonic mean	2.86	4.67

The arithmetic means of the two devices' capacities indicate that they have the same capacity. But device B is 50% "larger" than device A for benchmark 1, and 100% "larger" for benchmark 2. Device B is only 15% "smaller" than device A for benchmark 3. So, saying that they have the same capacity is not accurate.

You *could* use a weighted arithmetic mean, perhaps giving larger circuits higher weights. However, capacity measurements for each individual benchmark circuit are highly architecture-dependent, and circuits are not implemented the same way by different vendors. So getting vendors to agree upon a set of weights would be very difficult. A better way for computing a valid average capacity is by looking at resource utilization.

Using the following two alternatives, one being the inverse of the other, could provide a comparable metric for programmable-device "sizes."

Utilization measure:
$U_M=\Sigma(1/R_i)/n$ (average resources used per benchmark).

Capacity measure:
$C_M=n/\Sigma(1/R_i)$ (average number of repetition per device).

PREP's benchmark method repeats a simple, standardized circuit until no more will fit in the device under test. Therefore, if R_i is the repetition number of benchmark-circuit i, then $1/R_i$ is the portion of the device's resources that one instantiation of benchmark-circuit i uses up. And so $\Sigma(1/R_i)$ (for i=1 to n) is the portion of resources all n benchmark circuits use. And $\Sigma(1/R_i)/n$ is the average usage per benchmark circuit. The inverse of this average value is the average capacity measure.

Note that capacity measure is the *harmonic* mean of capacity measurements of individual benchmarks. Depending on the nature of your data, you can obtain a mean value three different ways: arithmetic mean, harmonic mean, or geometric mean. Although the properties of these three means come under the heading of elementary statistics, surprisingly few engineers apply them properly, so a review of a math text may be in order.

In this case, taking the harmonic mean of capacity benchmarks is reasonable because the numbers are rates (instantiation per device). The harmonic mean automatically provides higher weights to smaller numbers (ie, larger benchmark circuits). The harmonic means for devices A and B in **Table 1** are 2.86 and 4.67, respectively. Based on these numbers, device B has a larger overall capacity.

For a specific application, you can obtain a more accurate estimate by dividing a design into parts that match PREP's benchmark circuits. For example, suppose that a certain device's benchmark shows that it can accommodate 10 16-bit counters. If your application needs two 16-bit counters, they would occupy roughly 20% of the device. The total sum of all parts of the design should add up to somewhat less than 100% if you are trying to fit all the parts into one device.

Weighted-capacity measurements

The weighted harmonic mean embodies the weighted-capacity measurement. The weighted-capacity measure is

$$C_{WM}=\Sigma w_i/\Sigma(w_i/R_i) \text{ (for i=1 to n)}$$

where w_i is the weight you assign to benchmark i.

For example, if for a certain type of application the ratio for large state machines, 16-bit accumulators, and 4×4 ALUs is about 1:2:4, then the weights you assign to the respective PREP benchmarks can be simply 1, 2, and 4. You should give "unused" PREP benchmark circuits weights of zero.

For capacity comparisons, compute the weighted harmonic means for all candidate devices to determine the one with the best capacity for the given type of application. For a device to fit the application, its weighted harmonic mean must be greater than Σw_i. Note that if you replace Σw_i by 1 in the numerator, C_{WM} actually estimates the number of repetitions of the entire design which would fit into a given device. In this case, C_{WM} should be greater than, but close to 1 for a good capacity match between the device and your application.

Of course, you cannot properly match all real circuits with PREP's benchmark circuits. In these cases, you may have to use some "equivalence" estimations. For example, you may equate a 31-stage, linear-feedback shift register to two of PREP's 16-bit counters.

RENT'S RULE PROVIDES ANOTHER DEVICE METRIC

An interesting architectural measure is the logic-to-pin ratio. According to Rent's rule (an empirical equation relating I/O pins to circuits derived by IBM engineer E Rent):

$$I=k(C)^p$$

where I equals the number of I/O lines, C is the number of circuits, and k and p are positive constants.

For programmable devices, I is the number of user I/O pins and C is the number of usable gates. While various studies have produced different k and p values, generally p=0.5 is a good value to use for VLSI circuits (making the number of I/O pins proportional to the square root of the number of circuits). So, in

$$k=I/(C)^{0.5}$$

k turns out to be between 0.5 and 2.5 (mostly between 1 and 2) for programmable devices. Using k=1.5 as the dividing line, consider the device as having a high pin-to-logic ratio if k>1.5 and a high logic-to-pin ratio if k<1.5. In general, high pin-to-logic devices are good for I/O-intensive applications while high logic-to-pin devices are good for logic-intensive applications. Consequently, some PLD vendors produce devices having the same internal logic but with different numbers of I/O pins.

Another useful measure is the ratio between the number of registers (flip-flops) and the number of logic gates. In general, high register-to-logic devices are good for sequential applications and high logic-to-register devices are good for combinational applications.

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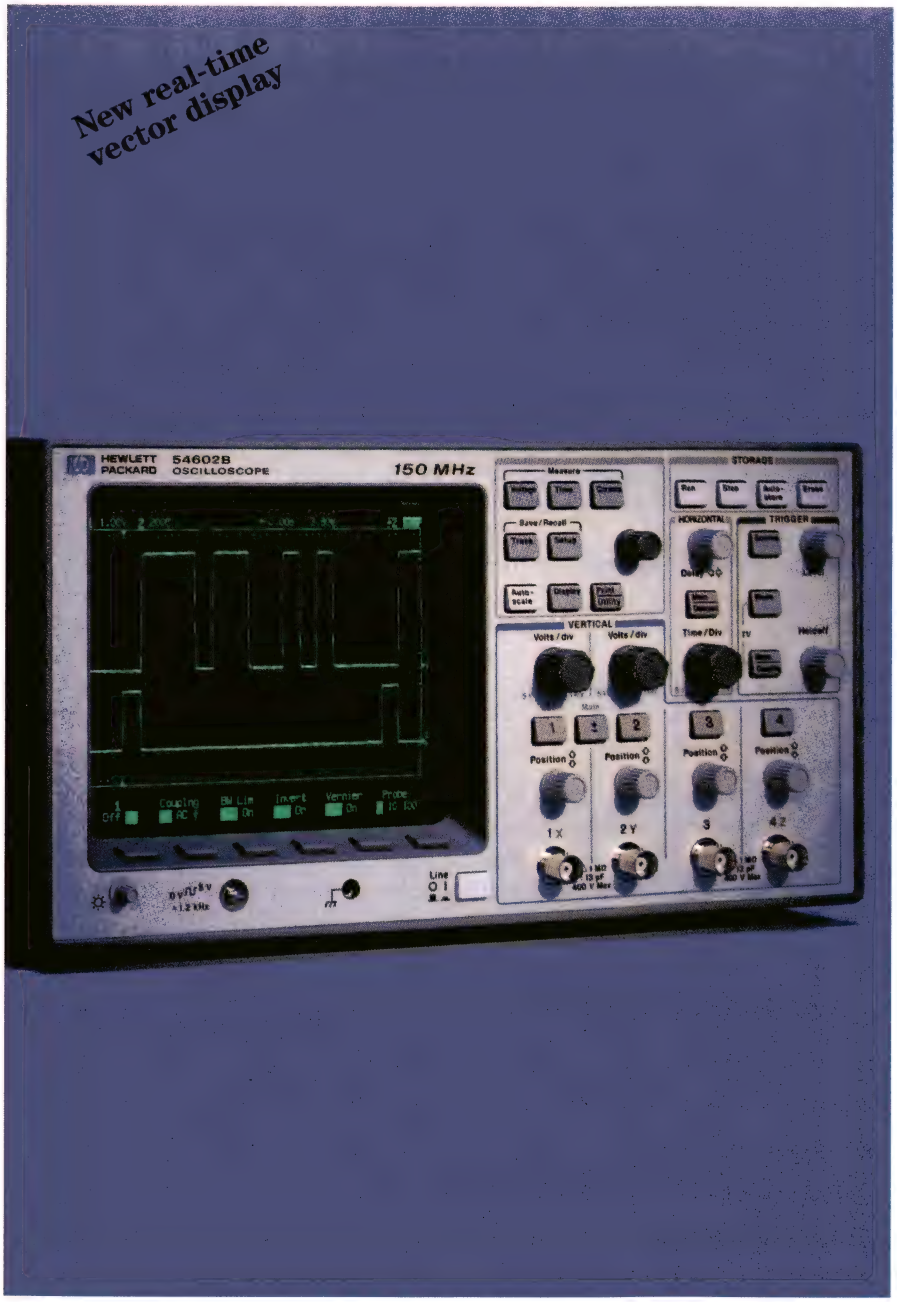

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CIRCLE NO. 122

Performance comparison

Again, the simple arithmetic mean is not a good measure of performance. In digital systems, the slower, lower frequency parts tend to dominate (limit) performance; hence, you should give them higher weights. The argument here parallels that for the capacity measure, the following two alternatives—one being the inverse of the other—can be used for programmable device speed.

Delay measure:

$T_M=\Sigma(1/f_i)/n$ (average delay per benchmark)

Performance measure:

$f_M=n/\Sigma(1/f_i)$ (average frequency for the device)

If f_i is the average frequency for benchmark i, then $1/f_i$ is the average delay for benchmark circuit i. And $\Sigma(1/f_i)$ (for i= 1 to n) is the total delay of n benchmark circuits. Therefore, $\Sigma(1/f_i)/n$ is the average delay per benchmark circuit. The inverse of this average value is the average frequency.

Because frequency benchmarks are also rates (cycles per second), the harmonic mean is reasonably the single performance measure. Note that the harmonic mean is always less than or equal to the arithmetic mean. The harmonic mean, in a way, incorporates a penalty for high variance. For a device with uniform performance results for the entire benchmark suite, the harmonic mean is the same as the arithmetic mean. On the other hand, for a device with varying benchmark results, the harmonic mean is always below the arithmetic mean. The wider the variation, the more the harmonic mean is below the arithmetic mean.

Again, for a specific design, you need only to examine numbers from benchmark circuits that match your design. For example, if the target design requires circuits similar to PREP's large state machine, a 4-bit ALU and a 16-bit counter at certain operating frequencies, then all candidate devices' results for these three benchmark circuits must exceed the respective target system's operating frequencies. Of course, your actual circuits are not going to be the same as benchmark circuits so use the benchmark result only as a first-order estimate.

Weighted harmonic performance mean

A weighted harmonic mean for performance makes no sense because, in general, you cannot trade the operating frequency of one part of the circuit with the frequency of another part. Often, the part of the circuit with the worst delay determines the design's overall performance in a synchronous system.

You may find examining the best and worst cases helpful to get some idea of the upper and lower bounds of performance. For example, using the critical-path design method, you could use the best-case result because the benchmark shows that achieving the reported speed by proper design is possible.

Some devices do not have all nine benchmark results reported because of vendors' inability to either implement or measure some of the benchmark circuits. Compute the harmonic means of these devices using the appropriately reduced n and using only available results. However, you should group these devices separately and flag their mean values to remind yourself and others that these values are not based on the entire benchmark suite.

Single-number comparison

The capacity-speed product is an option if you want a single figure of merit for capacity-performance comparisons. This number is the simple product of C_M and f_M, and "retz" (repetition-megahertz) can be the unit of measure. However, you must be aware that you cannot trade capacity for speed or vice versa as you can with the gain-bandwidth product for op amps. The capacity-speed product is only a figure of merit with which you can quickly eliminate unsuitable devices. For example, if an application requires a device to have 500 retz, then all devices with retz numbers less than 500 would not

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2. Swager, Anne, "Choosing complex PLDs and FPGAs," *EDN*, September 17, 1992, pg 74.
3. Small, Charles H, "Standardized [PREP] benchmarks peg big PLD's performance," *EDN*, January 21, 1993, pg 29.
4. Dingman, Sean, "Determine PLD metastability to derive ample MTBFs," *EDN*, August 5, 1991, pg 147.
5. Miller, Warren, "Design efficient state machines for PLDs or FPGAs," *EDN*, March 18, 1993, pg 225.
6. Small, Charles H, "FPGA conversion [to gate arrays]," *EDN*, June 6, 1992, pg 107.
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8. Quinnell, Richard A, "Application-tailored PLDs streamline designs, bring speed and lower cost," *EDN*, May 21, 1992, pg 81.
9. Conner, Doug, "Boost programmable logic performance with timing-driven tools," *EDN*, February 4, 1993, pg 47.
10. Small, Charles H, "Where CMOS rules, multiplexers slave," *EDN*, August 5, 1993, pg 57.
11. Conner, Doug, "EDN's hands-on FPGA project," *EDN*, April 9, 1992, pg 98, and *EDN*, April 23, 1992, pg 120.
12. Small, Charles H, "FPGA design methods, "*EDN*, August 5, 1991, pg 114.
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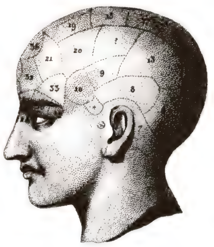

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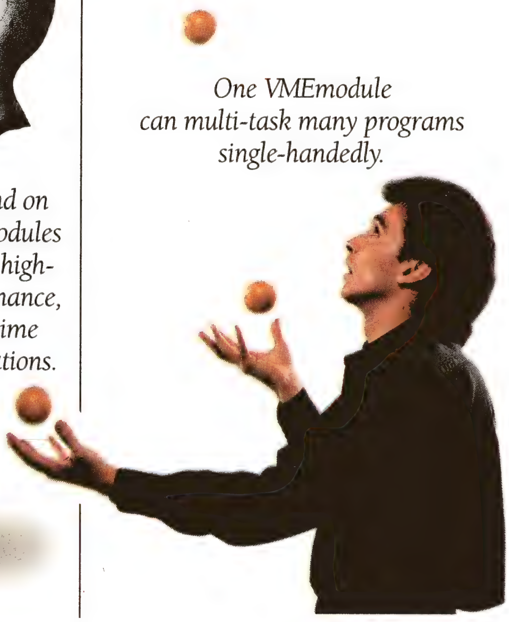

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qualify for the application. From among qualified devices, you then need to further qualify capacity and speed individually.

If you wish to include the cost in a single figure of merit, one way is the retz-per-dollar (rpd). That is, divide the retz number of the device by its cost. Thus, if a 500-retz device costs $100, then it is a 5-rpd device. However, device prices change regularly so be aware that rpd numbers can become outdated quickly.

> **The results of individual benchmarks are highly architecture-dependent.**

Additional information

Benchmark results also provide some idea about predictability of performance. A device with small differences between best- and worst-case frequencies has more predictable timing. Similarly, a device that permits a high number of instantiation of one particular benchmark circuit, but which is comparable or worse than other devices for other benchmark circuits, probably best suits applications similar to the particular benchmark circuit. The percent-fill numbers indicate whether the particular device architecture is amenable to the type of circuit the benchmark represents.

In any case, be aware of routing congestions, which can significantly reduce the number of usable logic cells. While digital designers usually have a good idea of timing and logic requirements early in the design, they do not have the slightest idea about the interconnection requirement, because this requirement depends highly on device architecture and implementation.

In summary, to use the benchmark results, first choose devices that are of comparable capacity (using either raw benchmark results, harmonic means, or weighted harmonic means) and big enough for the application. The next step is to choose, among candidate devices, ones that can satisfy the performance requirement (either raw benchmark results or harmonic means).

Obviously, you should give the highest priority to the critical parts of your design when looking at benchmark results. For example, if a critical part of your design is a high-speed counter, then the counter benchmark should weigh more than other benchmark results, and perhaps even be the determining factor. Do not mix benchmark results obtained under different conditions (ie, automatic vs manual routing or optimized for capacity vs optimized for speed).

Comments on prep benchmarks

Using PREP benchmarks to measure programmable devices is like running benchmark programs to measure computer performance. Even though some benchmark programs are extracts from real programs, real programs don't resemble these benchmark programs at all.

PREP benchmarks have the same problem: not enough benchmark circuits exist to represent all possible real design needs. PREP benchmarks are useful for applications similar to existing MSI circuits. They are small- to medium-sized circuits that are not necessarily useful for designing complex circuits such as video graphics.

Remember, also, that the results of individual benchmarks are highly architecture-dependent. Architecture dependency explains why a device can have higher capacity than others in one benchmark circuit but lower than others in another. CPLDs and FPGAs should use different benchmark suites because they differ from each other.

PREP's step-and-repeat method for filling up a device with repetition of the same basic circuit does not reflect real PLD applications. The step-and-repeat method emphasizes local interconnections and downplays global interconnections.

Since benchmarks do not address other real-life factors such as power consumption, number of I/O pins, output-drive capability, packaging, 3-state capability, testability, in-circuit programmability, etc, data books are still important sources of information.

The role of software in benchmark results introduces another complicating factor. Does the benchmark's results reflect the software tools or the expertise of the designer using the tools? Remember that versions 1.2 and 1.3 of PREP's benchmark results are different simply because tools changed. For example, some software can optimize a design, thus producing more-impressive benchmark results. Practitioners also disagree about just what constitutes "manual" routing.

Also, vendors may concoct devices or software specifically tailored to the benchmark circuits. Thus, a device may have high benchmark ratings yet yield poor results for real applications.

The computer industry has wasted considerable manpower on these improvements just to make inflated claims. What we really need is a universal design tool that allows designers to quickly benchmark devices using their actual designs.

In spite of these limitations, however, PREP benchmarks do provide some useful information. I hope future improvements will make them even more useful.

Reference

1. PREP Inc, 504 Nino Ave, Los Gatos, CA 95032. (408) 356-2169. FAX (408) 356-0195.

Author's biography

Sung C Hu has been a professor of electrical engineering at San Francisco State University for 14 years. In addition to teaching, he researches digital systems design, microprocessors, and computer architecture. He obtained his BSEE at California Polytechnic State University and his MS and PhD at Oregon State University. In his spare time he enjoys tennis, camping, and attending concerts.

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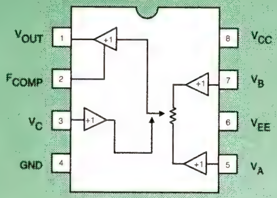

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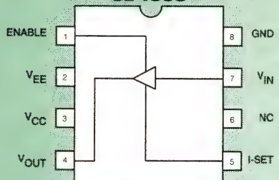

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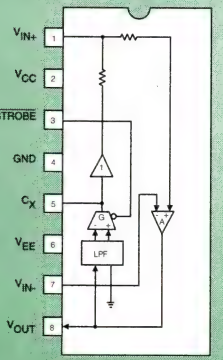

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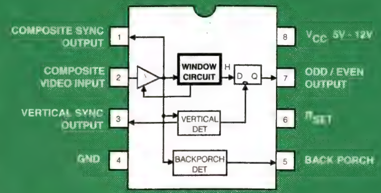

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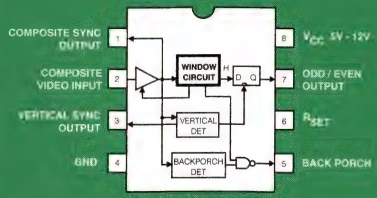

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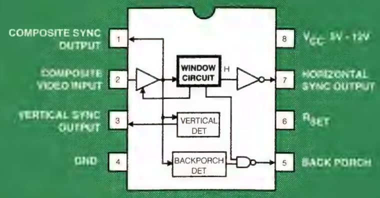

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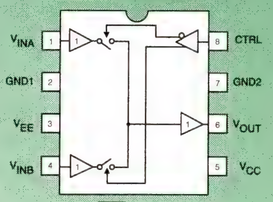

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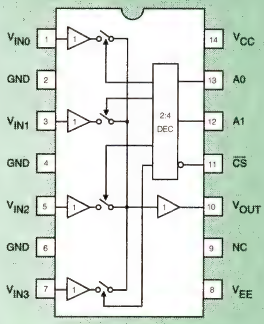

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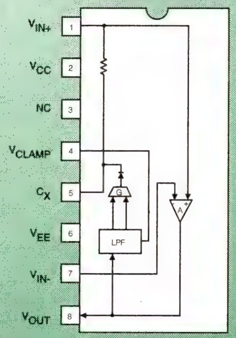

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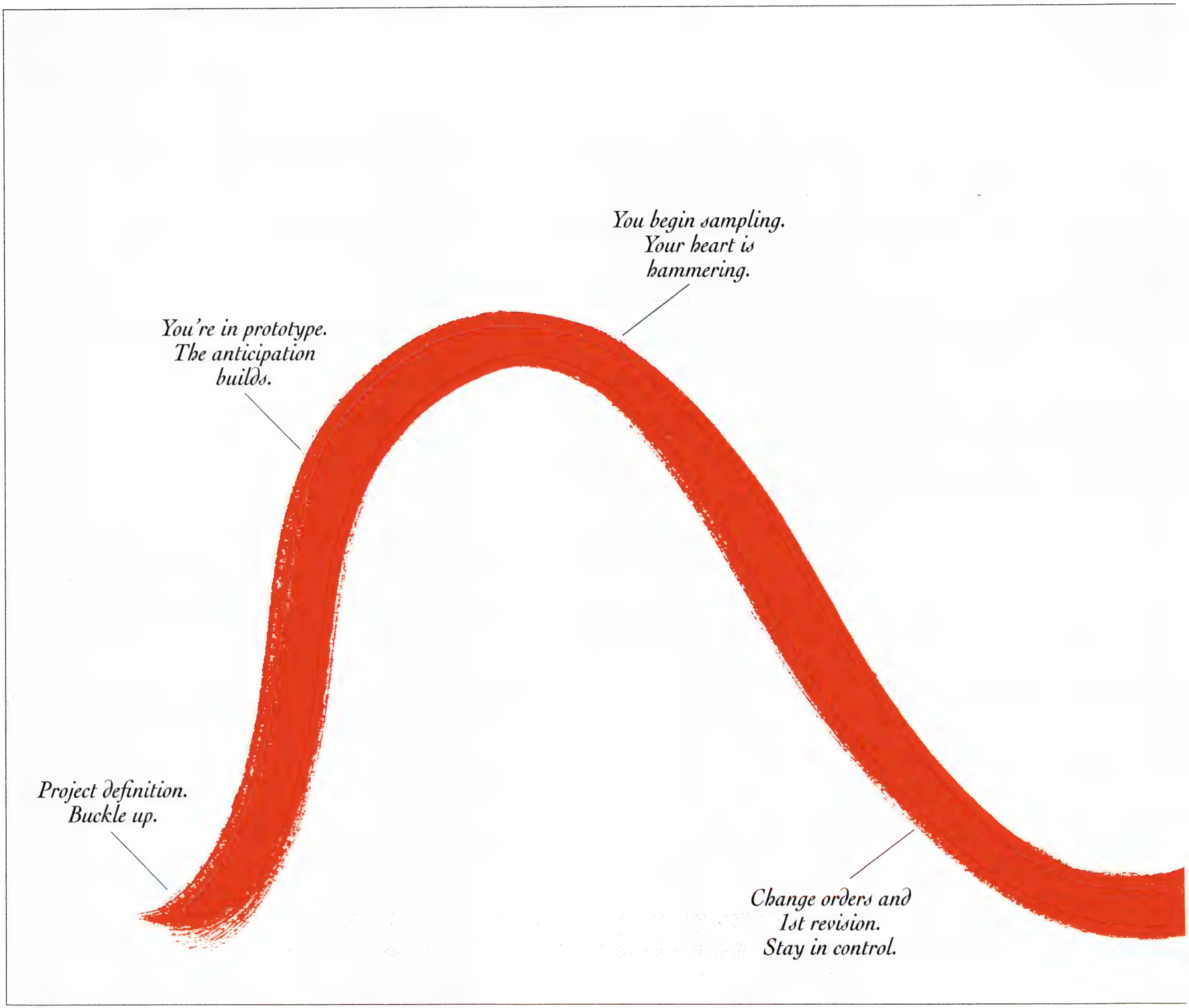
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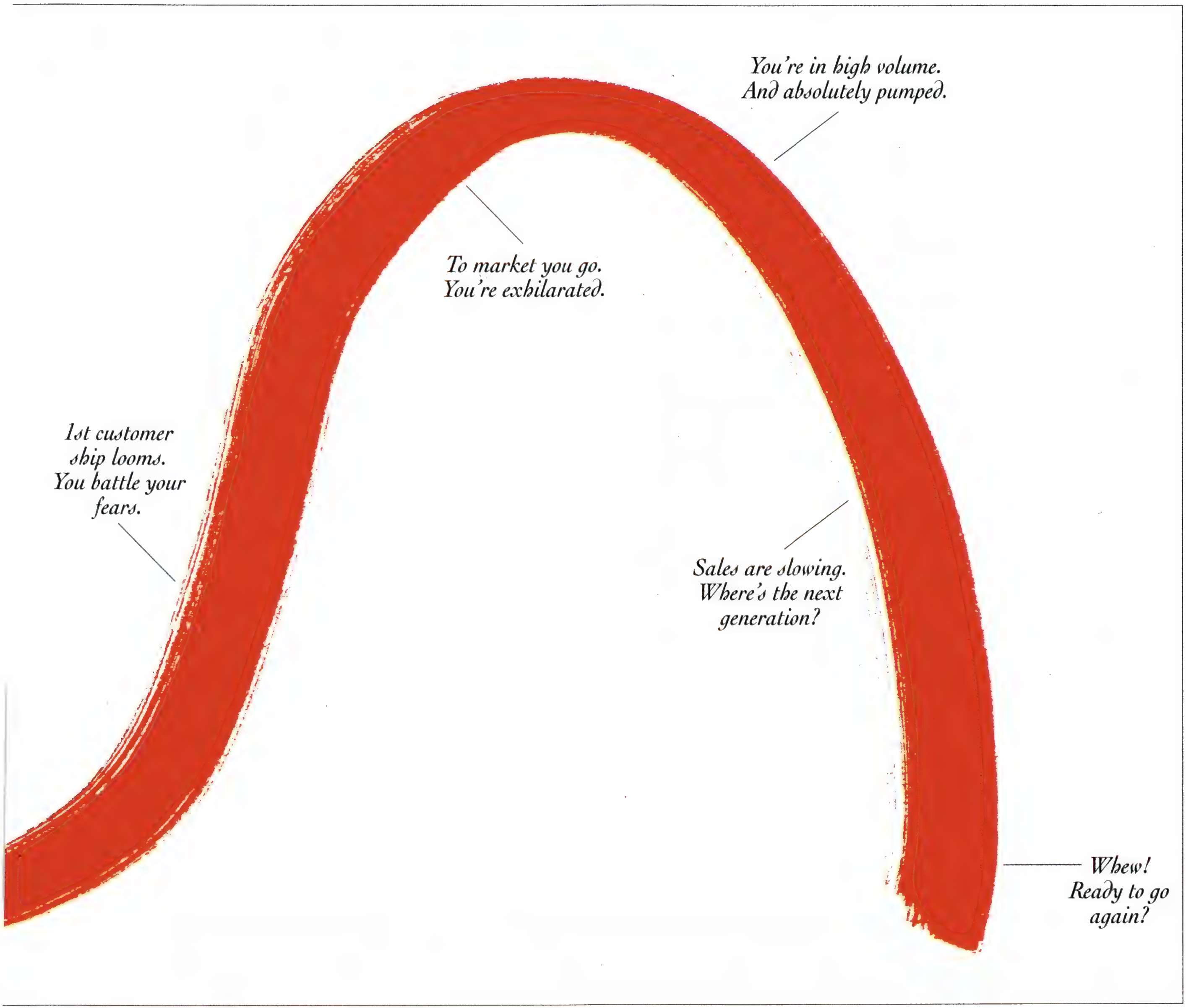
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Roger Crooks, Tektronix Inc

Embedded systems based on RISC µPs offer many advantages but present unique debugging challenges. Although a logic analyzer isn't the only tool you need to meet these challenges, it is an important one, and you should consider making it the cornerstone of your debugging strategy.

High-speed RISC (reduced-instruction-set computing) technology makes it practical to create embedded systems that previously would have been far too expensive and complex. Special-purpose chips (custom ASICs) enable these systems to deliver even greater performance at competitive prices. Although EDA (electronic-design automation) and CASE (computer-aided software engineering) tools make such complex designs possible, an inefficient debug environment can squander all of the time saved at the front end of the design process—particularly if the system under test contains a whole new class of complex debugging problems.

This article will help you to better understand the behavior of RISC-based systems in real-time applications and will show you how to get the most out of the instruments you use for analyzing and debugging those systems. The intended results are shorter and less painful product-development programs.

Most embedded systems handle some type of real-time input/output. The input may come from a disk drive, a robotics positioning sensor, an analog telecommunications link, or any device that is external to the embedded-system core. To function, the system's embedded software must not only be logically correct, it must also perform correctly in the time domain. That is, it must process the data in a specified amount of time. Most real-time embedded systems are also event driven—they are controlled by data they receive from external sources. Embedded systems' time-dependent nature makes debugging them especially difficult because many debugging tools ignore timing issues and provide information only on the software's logic.

Debugging in the time domain

In most cases, software designers initially debug their code on a workstation or a PC. Although this approach eliminates many logic errors, it is ineffective in debugging those features of a program that depend on hardware and time.

Because of the event-driven nature of real-time systems, debugging in the time domain requires monitoring of code as it executes. This usually requires instrumentation such as a logic analyzer or an in-circuit emulator. These tools are espe-

```
CACHE MEMORY
Loop_Begin_1
    Write FF to Test_Location_1 ___ TEST INSTRUCTION
   CODE
   CODE
   CODE
   CODE
   Goto Loop_Begin_1 else goto Loop2_Begin
Loop_Begin_2
    Write FF to Test_Location_2 ___ TEST INSTRUCTION
   CODE
   CODE
   CODE
   CODE
   Goto End else goto Loop_Begin_2
End
    Write FF to Test_Location_3 ___ TEST INSTRUCTION
```

Fig 1—This pseudo code indicates that embedding three instructions within two routines lets you use a logic analyzer for monitoring and timing analysis. The logic analyzer detects writes to unused memory locations, Test_Location_1, Test_Location_2, and Test_Location_3. By writing specific values to a single test address and triggering on values of interest, you can reduce the test address requirements to one location.

cially effective for analysis of time-critical functions. Many of these instruments offer additional tools that allow timing analysis, performance analysis, or time-domain triggers. Time-oriented triggering may include triggering on minimum pulse widths or triggering when multiple counter/timers overflow, revealing that a routine has not finished executing in a specified time.

A real-time trace buffer that captures aspects of the program's execution history is an effective tool for finding elusive problems in event-driven systems. The deeper the trace buffer, the better. Deep trace lets you look back in time to find the cause of problems. Often, problems don't show up until some time after the event that precipitates them. Because of RISC processors' limited instruction sets, high-level code compiles into more RISC machine-language instructions than CISC (complex-instruction-set computer) instructions. Although the RISC version of a program may execute faster, it usually takes more bus cycles, necessitating a deeper trace buffer.

Whereas many of the techniques discussed here apply to both RISC and CISC designs, developers who use RISC chips generally face more architectural issues. These characteristics include

- very large caches, secondary caches, and deep pipelines,
- clock rates exceeding 30 to 50 MHz,
- the presence of other special-purpose μPs,
- dense packages with hundreds of pins and very narrow pin spacing,
- large numbers of registers or register sets,
- a limited set of simpler instructions, and
- programs written in high-level languages rather than in assembly language.

To understand their impact on debugging, you should examine each of these aspects separately.

Primary and secondary caches and pipelines

Analyzing system behavior with the caches turned on can obscure a debugging tool's view of actual performance. Turning caching off allows logic analyzers and emulators to disassemble correctly and provides a better view of the code being executed—but changes the system characteristics, possibly masking real problems. Debug monitors can run with caches on, but when they hit a breakpoint, the cache is flushed, and its contents are lost—again changing the real operation of the system. You should debug a routine in two passes. In the first pass, turn the cache off and debug the routine's logic. On the second pass, turn the cache back on and ensure that the timing is correct.

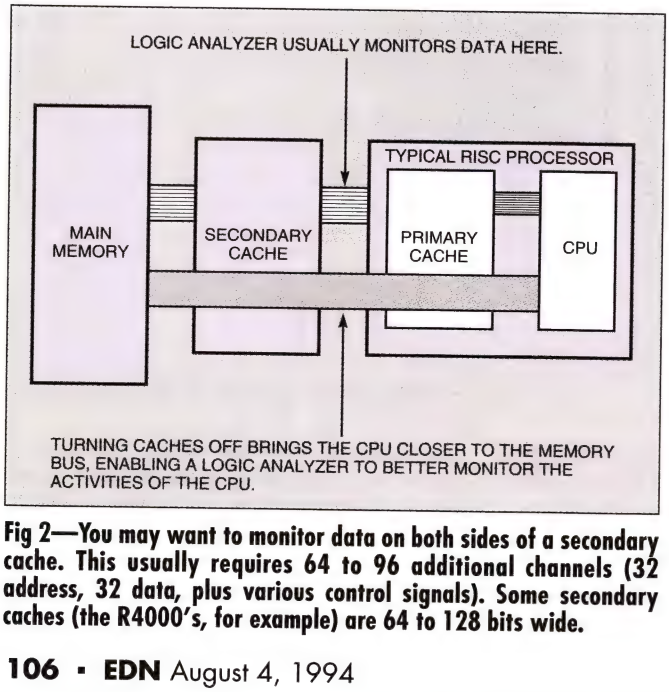

LOGIC ANALYZER USUALLY MONITORS DATA HERE.
MAIN MEMORY
SECONDARY CACHE
TYPICAL RISC PROCESSOR
PRIMARY CACHE
CPU
TURNING CACHES OFF BRINGS THE CPU CLOSER TO THE MEMORY BUS, ENABLING A LOGIC ANALYZER TO BETTER MONITOR THE ACTIVITIES OF THE CPU.

Fig 2—You may want to monitor data on both sides of a secondary cache. This usually requires 64 to 96 additional channels (32 address, 32 data, plus various control signals). Some secondary caches (the R4000's, for example) are 64 to 128 bits wide.

One way to verify the timing of a routine that executes from cache is to instrument the code with an instruction that lets you see what is happening. If you insert memory-write instructions into a critical routine that executes from cache, you can set up a logic analyzer to time the event and to monitor the memory location being written to or simply to monitor the progress of the routine's execution. You can enhance this technique by writing various values, such as the address of the routine and the value of a key register, to the specified memory location. This approach allows more flexible triggering, qualification, and display (**Fig 1**).

Another factor relates to context switching: The cache usually must be flushed and refilled before a new routine can start executing. To speed such switching, some RISC chips allow disabling the cache so that the program runs directly out of main memory. This is a dangerous practice. Although it may speed the context switch, it could reduce the overall speed of the interrupt handler, which now must run directly out of main memory.

Secondary caches add another level of complexity. You must carefully control the two caches to make sure that no data are lost and that each cache remains filled with the correct data (that is, the caches must maintain coherency). A logic analyzer with enough channels can monitor the input to both caches and verify that the correct data are being loaded into each cache at the proper time (**Fig 2**).

Another difficult debugging chore is verifying burst-mode operations. Burst mode is a fast way to move data from main memory to cache. Rather than issuing an address for each memory location, burst mode issues a starting address and fetches data from sequential memory locations. This reduces the execution overhead because additional addresses need not be sent over the bus. Debugging burst-mode hardware requires an instrument fast enough to acquire the burst data

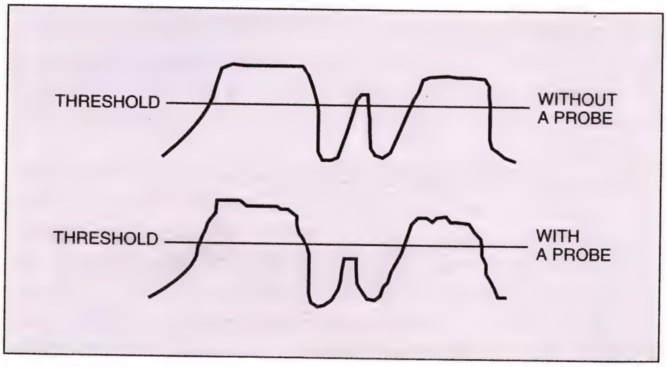


Fig 3—A probe with high capacitive loading absorbs energy from the signal and changes its characteristics, sometimes masking problems.

and to reconstruct the entire sequence in either hardware or software. If the instrument is not fast enough, the missing data keeps it from displaying an accurate picture of the program execution. Instruments with inadequate speed accurately display only the first instruction of a burst.

Faster clock rates

Although fast clocks result in fast software execution, they can cause tremendous problems in hardware. Clock rates approaching 50 MHz require designers to consider each signal and every physical path with care. RISC clocks, which have rise times as short as 1 nsec, cause problems that are very difficult to isolate.

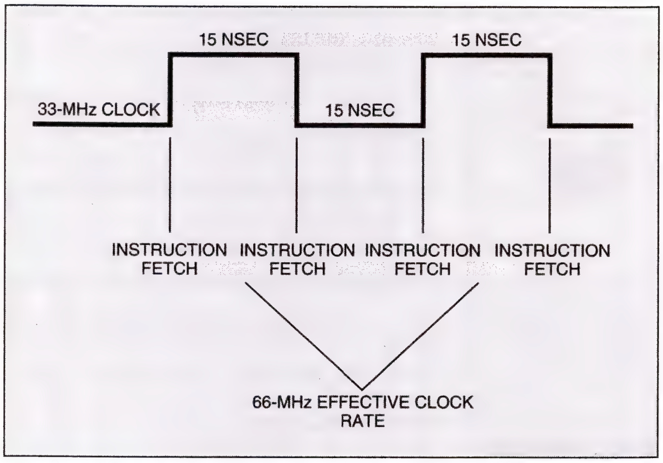


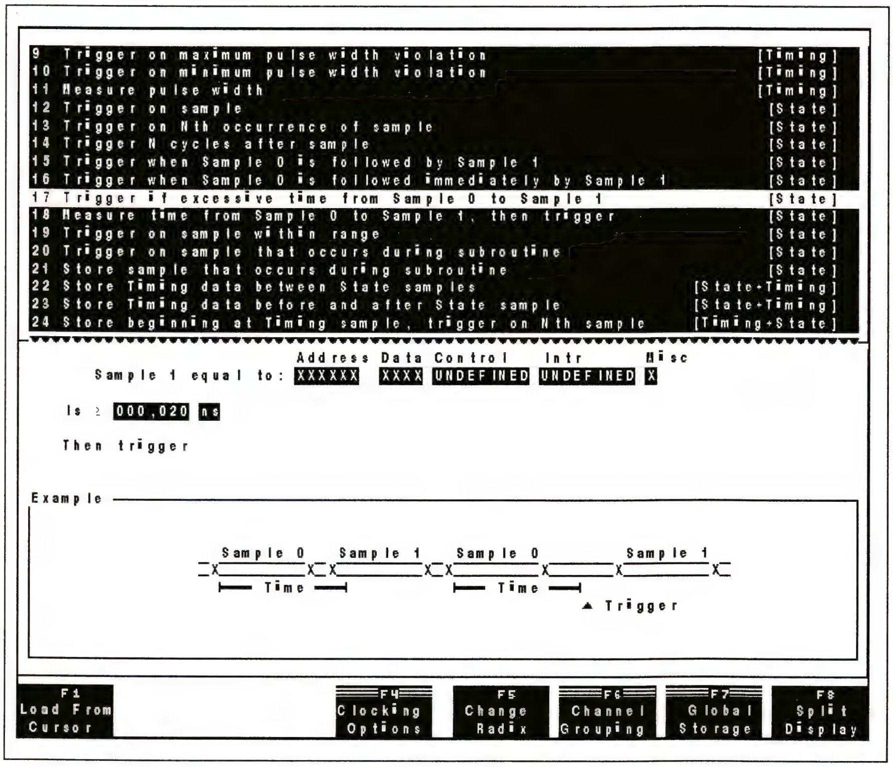
Fig 4—When a RISC μP fetches instructions on both edges of the clock, the effective clock rate doubles, requiring a logic analyzer that can acquire state data at the doubled clock rate (66 MHz in this example).

High clock rates can result in crosstalk—causing noise on physically close signal lines. When a location is suspect, one approach is to cut the signal lines in question and reroute them outside the area of concern. This work-around may cure the crosstalk, but it introduces other problems, such as uncontrolled impedance and changes in the signal characteristics. Further, improper termination of fast signals can cause reflections that, when large enough, can change the input characteristics of devices along that signal line. In all of these cases, attaching a scope or logic-analyzer probe to the suspect line can change the characteristics of the signal and cause the problem to vanish, resulting in extreme frustration (**Fig 3**).

To accurately debug problems of these types, you need advanced probing systems. When working with RISC technology, you need oscilloscope and logic-analyzer probes that introduce low capacitive loading. Such probes have minimal impact on signal characteristics and let you track down real problems instead of phantoms caused by your instruments.

Besides clocking at high rates, some RISC processors fetch data at both edges of the clock (two instructions per cycle). This effectively doubles the clock rate at which instruments must acquire data and trigger (**Fig 4**).

Slower clocks allow enough time for signals to propagate through interconnecting cables and sockets. As signals speed up, a design's margin for propagation delays (the time for a signal to get from one area of a board to another) decreases. In synchronous systems, each device has a setup-and-hold-time specification. As signal speeds increase, setup-and-hold time shrinks, and signal skew (the difference among the arrival times of the same signal—or supposedly simultaneous signals—at different points) requires closer scrutiny.



```
9  Trigger on maximum pulse width violation                              [Timing]
10 Trigger on minimum pulse width violation                              [Timing]
11 Measure pulse width                                                   [Timing]
12 Trigger on sample                                                      [State]
13 Trigger on Nth occurrence of sample                                    [State]
14 Trigger N cycles after sample                                          [State]
15 Trigger when Sample 0 is followed by Sample 1                          [State]
16 Trigger when Sample 0 is followed immediately by Sample 1              [State]
17 Trigger if excessive time from Sample 0 to Sample 1                    [State]
18 Measure time from Sample 0 to Sample 1, then trigger                   [State]
19 Trigger on sample within range                                         [State]
20 Trigger on sample that occurs during subroutine                        [State]
21 Store sample that occurs during subroutine                             [State]
22 Store Timing data between State samples                         [State+Timing]
23 Store Timing data before and after State sample                 [State+Timing]
24 Store beginning at Timing sample, trigger on Nth sample         [Timing+State]

                          Address Data Control    Intr       Misc
      Sample 1 equal to:  XXXXXX  XXXX UNDEFINED  UNDEFINED  X

    Is ≥ 000,020 ns

    Then trigger
```

Fig 5—The logic analyzer triggers to measure a setup-and-hold violation. Preprogrammed trigger setups simplify complex measurements.

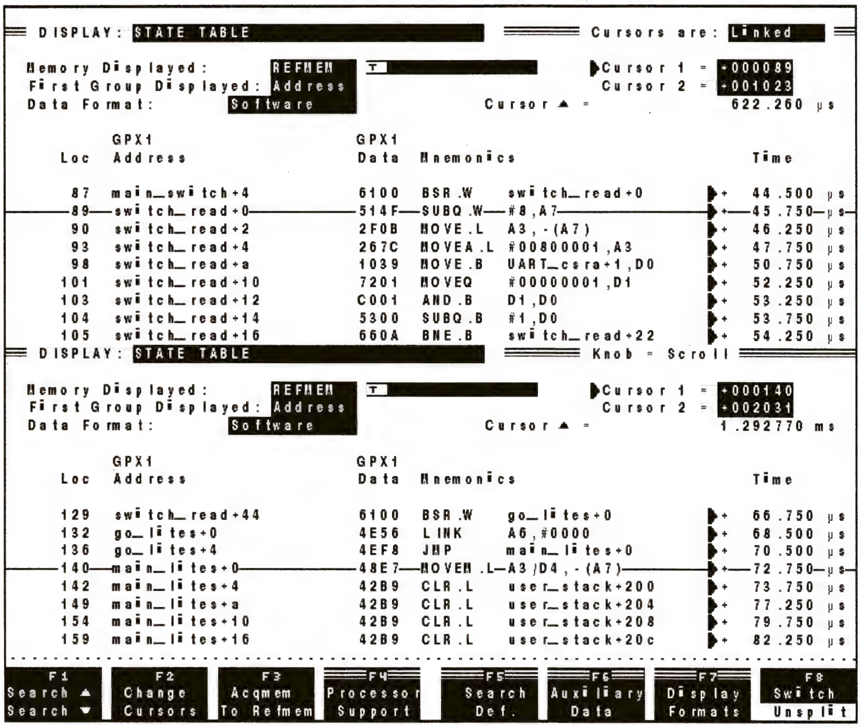
When a device's setup-and-hold times are "on the edge," metastability is a common problem. Monitoring signals to detect skew-related problems requires a fast oscilloscope or an accurate logic analyzer with resolution of 1 to 2 nsec. Be sure that the channel-to-channel skew specifications of the instrument do not mask the actual skew in the system. Also, look for a logic analyzer that can measure setup-and-hold violations. It should offer low capacitive loading and fast triggering (**Fig 5**).

Designs with multiple processors

Many embedded systems now incorporate multiple processors in a redundant architecture, a master-slave configuration, or a parallel-processing scheme. Special-purpose μPs like DSPs are usually paired with a fast CPU to perform complex operations such as real-time data acquisition and processing. Although modern RISC and CISC architectures enable multiple processors to work together with relative ease, few debugging tools have kept pace with multiple-processor designs. A modern logic analyzer can be extremely valuable in multiprocessor systems.

Many recently introduced logic analyzers can monitor and time-correlate the activity of multiple processors. The analyzers perform time-correlation of multiple µPs by time-stamping data as the acquisition system gathers it. The more accurate the time stamp, the better the correlation. Look for time stamps with resolutions of 10 nsec or finer (100 MHz or higher).

Logic analyzers with split-screen displays can show the behavior of any two processors at one time. Analyzers with a "link-cursor" feature allow you to scroll one display while the second scrolls in perfect time alignment. Using this feature lets you monitor how one processor passes data to another and verify that redundant systems are actually executing in synchronism. In parallel systems, monitoring processing time helps you to balance the computing load among the processors. A common problem in multiprocessor systems is stale data in caches. Logic analyzers can help pinpoint this problem (**Fig 6**).



```
DISPLAY: STATE TABLE                                    Cursors are: Linked

 Memory Displayed:        REFMEM  T                     Cursor 1 = +000089
 First Group Displayed:   Address                       Cursor 2 = +001023
 Data Format:             Software             Cursor ▲ =          622.260 µs

        GPX1                       GPX1
   Loc  Address                    Data  Mnemonics                        Time

    87  main_switch+4              6100  BSR.W     switch_read+0      +   44.500 µs
    89  switch_read+0              514F  SUBQ.W    #8,A7              +   45.750 µs
    90  switch_read+2              2F0B  MOVE.L    A3,-(A7)           +   46.250 µs
    93  switch_read+4              267C  MOVEA.L   #00800001,A3       +   47.750 µs
    98  switch_read+a              1039  MOVE.B    UART_csra+1,D0     +   50.750 µs
   101  switch_read+10             7201  MOVEQ     #00000001,D1       +   52.250 µs
   103  switch_read+12             C001  AND.B     D1,D0              +   53.250 µs
   104  switch_read+14             5300  SUBQ.B    #1,D0              +   53.750 µs
   105  switch_read+16             660A  BNE.B     switch_read+22     +   54.250 µs
DISPLAY: STATE TABLE                                    Knob = Scroll

 Memory Displayed:        REFMEM  T                     Cursor 1 = +000140
 First Group Displayed:   Address                       Cursor 2 = +002031
 Data Format:             Software             Cursor ▲ =        1.292770 ms

        GPX1                       GPX1
   Loc  Address                    Data  Mnemonics                        Time

   129  switch_read+44             6100  BSR.W     go_lites+0         +   66.750 µs
   132  go_lites+0                 4E56  LINK      A6,#0000           +   68.500 µs
   136  go_lites+4                 4EF8  JMP       main_lites+0       +   70.500 µs
   140  main_lites+0               48E7  MOVEM.L   A3/D4,-(A7)        +   72.750 µs
   142  main_lites+4               42B9  CLR.L     user_stack+200     +   73.750 µs
   149  main_lites+a               42B9  CLR.L     user_stack+204     +   77.250 µs
   154  main_lites+10              42B9  CLR.L     user_stack+208     +   79.750 µs
   159  main_lites+16              42B9  CLR.L     user_stack+20c     +   82.250 µs
```

Fig 6— Two µPs are being monitored. A time-stamp correlates the two displays. The linked-cursors feature lets you scroll one display and keep the second display perfectly aligned.

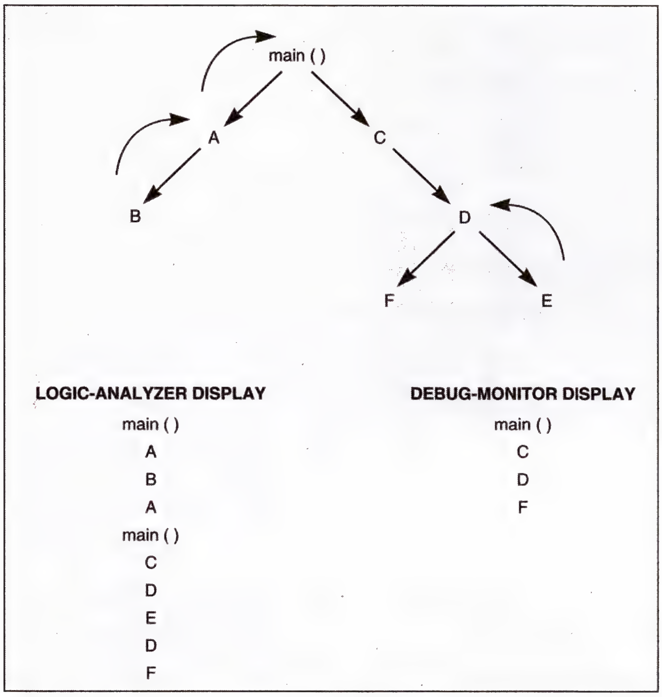


Fig 7—As functions are executed, a debug monitor loses information. For example, it loses track of subroutines that have been called but haven't finished executing. The logic analyzer provides a complete history of execution.

High-level languages and code optimization

Many designers of embedded systems write time-critical routines in assembly language. This approach provides absolute control over what is happening in a system and allows better control over hardware. But RISC µPs are nearly impossible to program in assembly language because of their large number of registers, their limited number of instructions, and their need for code optimization. Of these problems, code optimization is the most difficult to handle.

As a result, development-tool suppliers have put a great deal of effort into the design of optimizing compilers for RISC µPs. Traditional code-optimization techniques include peephole optimization and the elimination of dead and redundant code. Some optimizing compilers speed loop-routine execution by analyzing loop code and moving nonessential code outside the loop. Compiler designers understand such techniques fairly well, but RISC presents unique problems.

To achieve the optimum RISC performance, the compiler rearranges the machine-language instructions' execution order. The idea is to take advantage of the µP's architecture to help achieve the goal of executing one or more instructions per cycle. Without this optimization, performance suffers.

Optimization takes place in two stages. The compiler is run once and the output is evaluated. During the second stage, instructions are reordered to keep the execution unit working full time. This analysis is complex and, in some cases, may be incorrect. Often, a compiler bug occurs only with a specific sequence of instructions; changing the execution order

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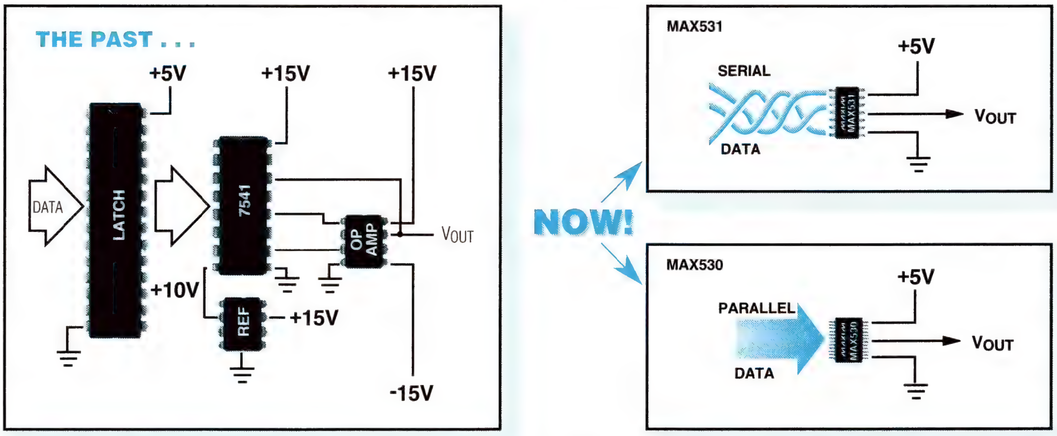

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can make the error disappear. Because of the sheer number of possible combinations, it is practically impossible for a compiler vendor to test them all.

When things should work but don't, you can use a logic analyzer to monitor the actual assembly instructions in the vicinity of the problem code. Careful analysis of the execution trace helps to determine if there is indeed a compiler bug. Compiler vendors, once informed of the specifics of a

COST-EFFECTIVE DEBUG WITH ENTERPRISE INSTRUMENTATION

Combining logic analyzers and software debug tools works well if you can integrate the tools in your engineering environment. This is the basic concept behind Tektronix's Enterprise Instrumentation strategy. By employing the network capability on the DAS and TLA families of logic analyzers, users can easily implement the strategy outlined in the article and shown in **Fig A**.

Enterprise instrumentation requires two fundamental capabilities:

- remote control of instrumentation over a LAN and
- the ability to share data between development and debug tools.

With remote control, a developer at a workstation can set up and run a logic analyzer, display the results, monitor the prototype that is being debugged, and apply stimuli to it. The ability to control the prototype is critical during debugging, as you frequently need to reset the prototype or generate an interrupt. With Tektronix's 92PORT tool, you can stimulate eight lines and monitor eight lines on your prototype via a LAN.

It is often difficult to correlate the data acquired from a logic analyzer with what is happening in the software. You have to refer to a link map to translate an address to a location in the high-level program. With a link between the compiler and the logic analyzer, you can view the actual compiler function names in the logic-analyzer display. Tektronix's LA-Connect program provides links between most compilers and Tektronix logic analyzers.

Currently two LA-Connect vendors, Concurrent Sciences Inc and Microtec Research, provide suites of high-level debuggers, debug monitors, compilers, and links to other vendors' compilers. These tools coupled with Tektronix logic analyzers, enable you to put together a comprehensive and cost-effective development environment for today's latest and most powerful μPs. These environments can reside on a variety of PCs and Unix workstations.

How the link works

The keys to an effective hardware/software debug environment are protocols that link design information to the logic analyzer. Converter programs can extract symbolic information from the compiler's output (object module) and download the data to the logic analyzer. The advantage of linking to the object module rather than to the compiler or debugger itself is that object-module formats are essentially language-independent. IEEE-695, COFF, OMF86, OMF386, and Extended TekHEX are examples of popular object-module formats and load modules used with various μPs and languages such as C, C++, Ada, and Pascal.

The benefit of this strategy is that all of these tools already exist in most organizations. The hardware group probably use a logic analyzer to debug the hardware, and the software group probably has the source-level debugger and debug monitor. Knowing how to link these tools effectively and use them throughout the design is the key to a cost-effective and productive design-team environment (**Fig B**).

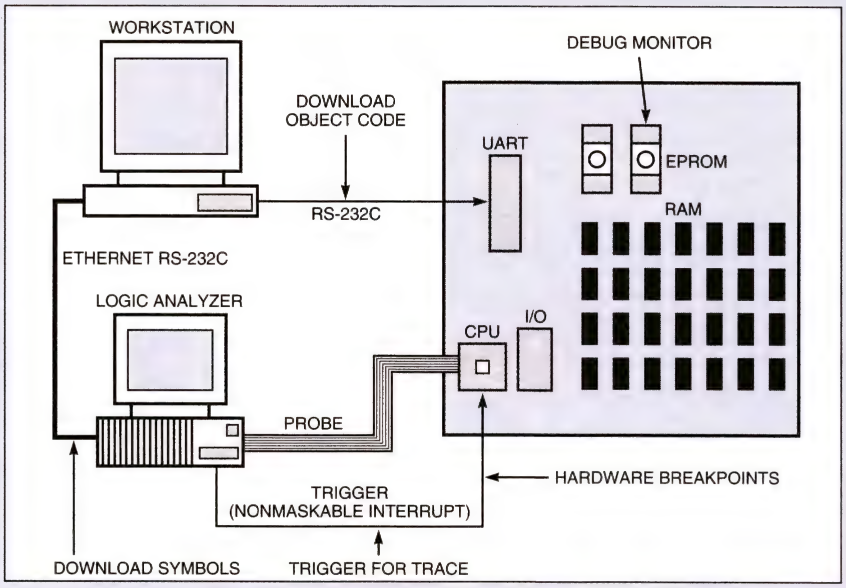

Fig A—LA-Connect and Enterprise Instrumentation provide a modern, cost-effective, networked-based hardware/software debug environment.

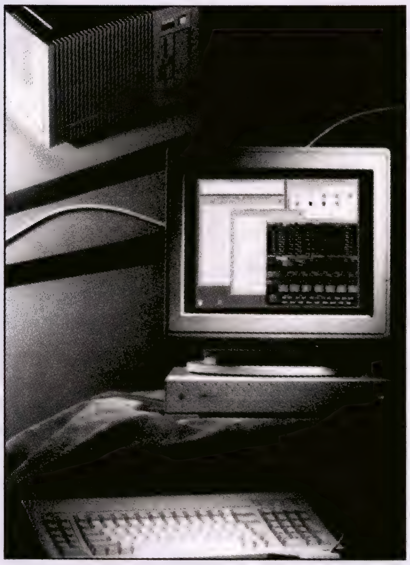

Fig B—From a networked workstation, a user can switch among tools and view acquired data on a single screen. A workstation running Microtec Research's Xray debugger controls a DAS 9200 system.

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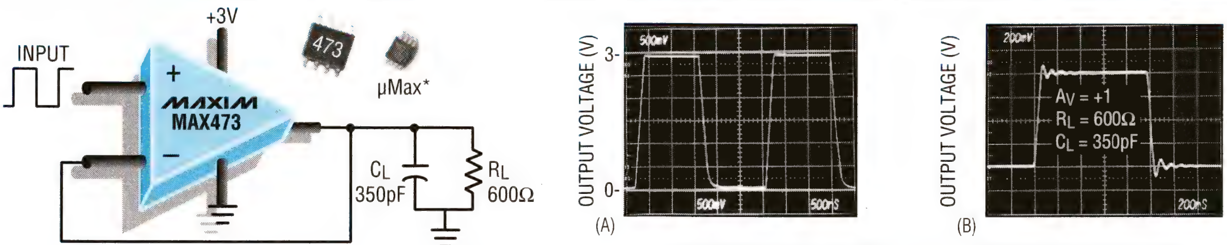

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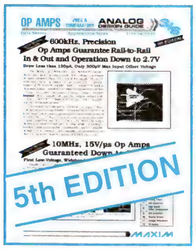

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CIRCLE NO. 82

problem, can quickly correct the compiler or formulate a way to work around the bug.

Superscalar processors do not present too many unusual debugging problems, but they can greatly impact the compiler. Just as a compiler must reorder instructions for a deep pipeline, it must do the same for a superscalar processor. The goal for code optimization in both types of architectures is to keep the processor executing one instruction or more per clock cycle while avoiding unnecessary branches or breaks in program flow. These breaks cause pipeline stalls, which slow throughput.

Software and hardware breakpoints

Debugging real-time embedded systems requires a high-level-language debugger with both software and hardware breakpoints as well as real-time trace. Software breakpoints stop program execution just before the execution of an instruction. These breakpoints are usually implemented by replacing the target instruction with a trap that transfers control to a debugger—usually a debug monitor or an emulator. When execution resumes, the actual instruction is inserted back where it was and is executed. Caches or deep pipelines do not affect software breakpoints, because the breakpoints stop execution when the instruction arrives at the CPU.

Because deep pipelines and caches are common in the RISC world, using software breakpoints is especially effective when debugging code execution. Although a logic analyzer cannot generate a software breakpoint by itself, teaming a logic analyzer with a debug monitor results in a powerful combination. (See **box**, "Cost-effective debug with enterprise instrumentation.")

Hardware breakpoints, on the other hand, are essential for debugging ROM-based programs or when it is necessary to stop on data reads or writes. Hardware breakpoints require some type of instrumentation—either a logic analyzer or an emulator—to monitor the address and data buses. When the instrument detects the desired event, it generates a trigger, which causes control to pass to the debug monitor. (An emulator stops the processor directly.) Hardware breakpoints usually work well with caches because most caches are set up to be bypassed on a data read or write; thus, data reads and writes usually are seen on the same bus cycle as the actual instruction.

With RISC chips, the deep caches and pipelined architectures cause long delays between instruction fetches and execution. These delays make hardware breakpoints ineffective. Often the cache is flushed before the instruction is even executed. Most logic analyzers and emulators work best with the cache turned off. But this changes the operating characteristics of the system and may mask some time-dependent bugs. Efficient debugging requires a combination of both hardware and software breakpoints.

Problems with large numbers of registers

Large numbers of internal registers increase the time needed to do a context switch. This problem occurs because more registers have to be saved on the stack. Even in architectures, such as SPARC, that have register windows, the state of the processor must eventually be saved. When the original routine resumes, register data are retrieved from the stack, and execution continues. Since context-switching time is critical in many embedded systems, you can be tempted not to save all of the registers, but this approach adds another level of complexity to the verification effort. You must make sure that all of the needed registers are saved and that no routine uses a register that is not saved. In an event-driven system, you cannot always control the flow of events, so careful management of the stack is critical.

Errors often occur as a result of context switching. Although you can easily debug errors in saving and restoring registers, more elusive problems occur with nested routines. Each context switch pushes data onto the stack. When a return is executed, the data are fetched from the stack and the stack pointer is moved. Nested routines cause the stack to grow, and if you have not allocated sufficient space to the stack, the stack can grow into the code or data space and corrupt the program.

Another type of stack problem is improper handling of the stack pointer. An off-by-one error is a common problem that causes the stack to grow gradually until it overflows (a memory leak). This type of problem appears randomly because it depends upon how the program executes. Stack-pointer errors that occur when data are pushed onto the stack do not show up until the data are popped back off.

A logic analyzer is an efficient tool for debugging a stack-overflow problem. Setting a range recognizer to monitor the valid stack space causes the logic analyzer to trigger if the stack grows outside this address range. In addition to detecting the event, a logic analyzer can look at a trace of the context switch and determine what code caused the stack to overflow. Debug monitors that show a trace of subroutine calls leading up to a breakpoint see forward calls only to subroutines that haven't returned (that is, ones that haven't completed execution). In contrast, a logic analyzer shows a complete history of execution (**Fig 7**).

Hardware and software debugging go hand in hand with the design of RISC-based systems. Understanding RISC technology's inherent problems and the tools available to fix them helps you to get your product to market faster. Effective debugging of RISC-based systems starts with selecting the right instrumentation and the most effective debug strategy. EDN

Author's biography

Roger Crooks is a program manager responsible for designing and marketing logic-analysis systems at Tektronix Inc in Beaverton, OR. He has worked at Tektronix for 15 years and on logic analyzers for five years. He holds a BSEE from Purdue University, West Lafayette, IN, and an MBA from the University of Portland, Portland, OR. His hobbies are skiing and bicycling.

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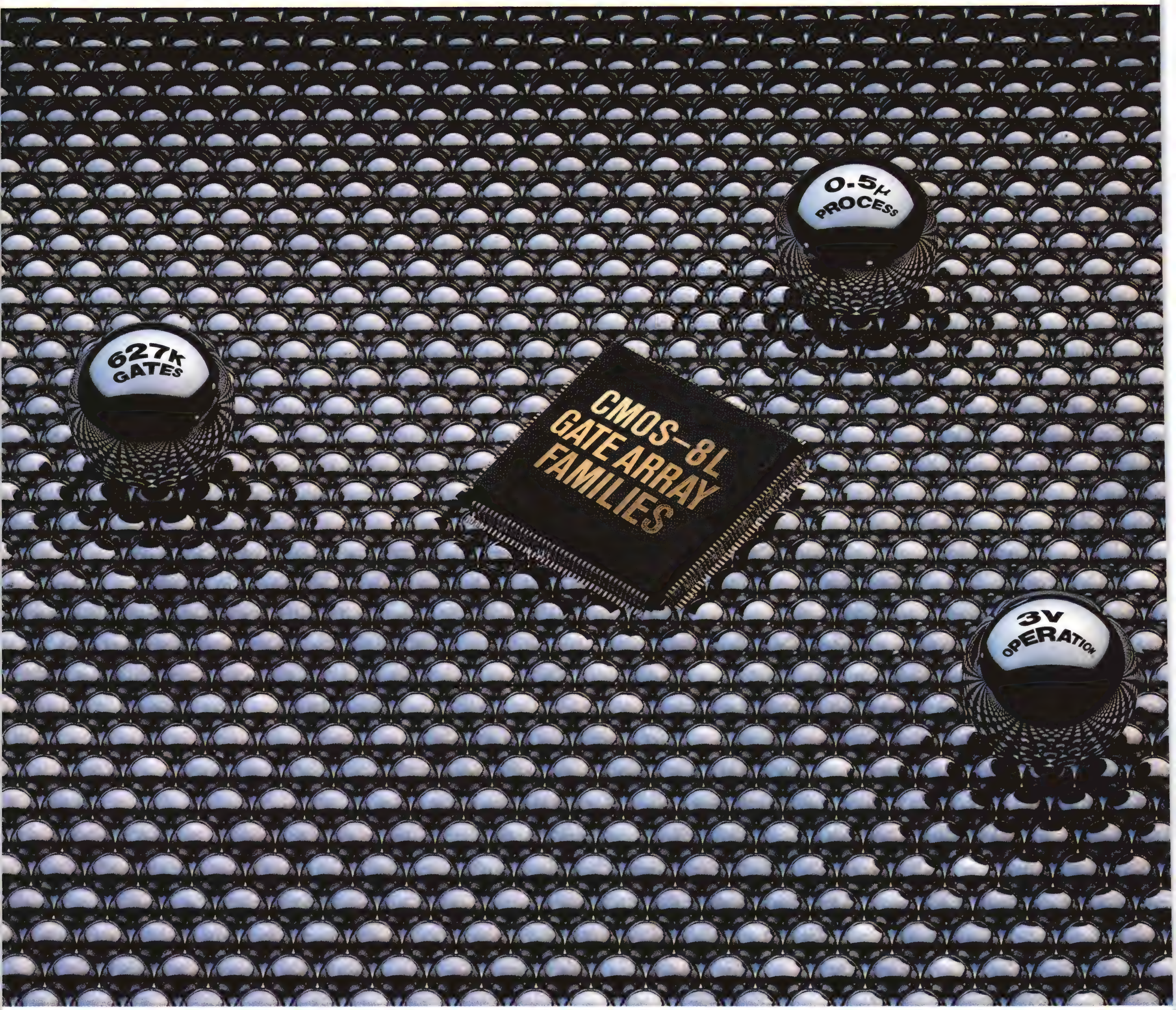

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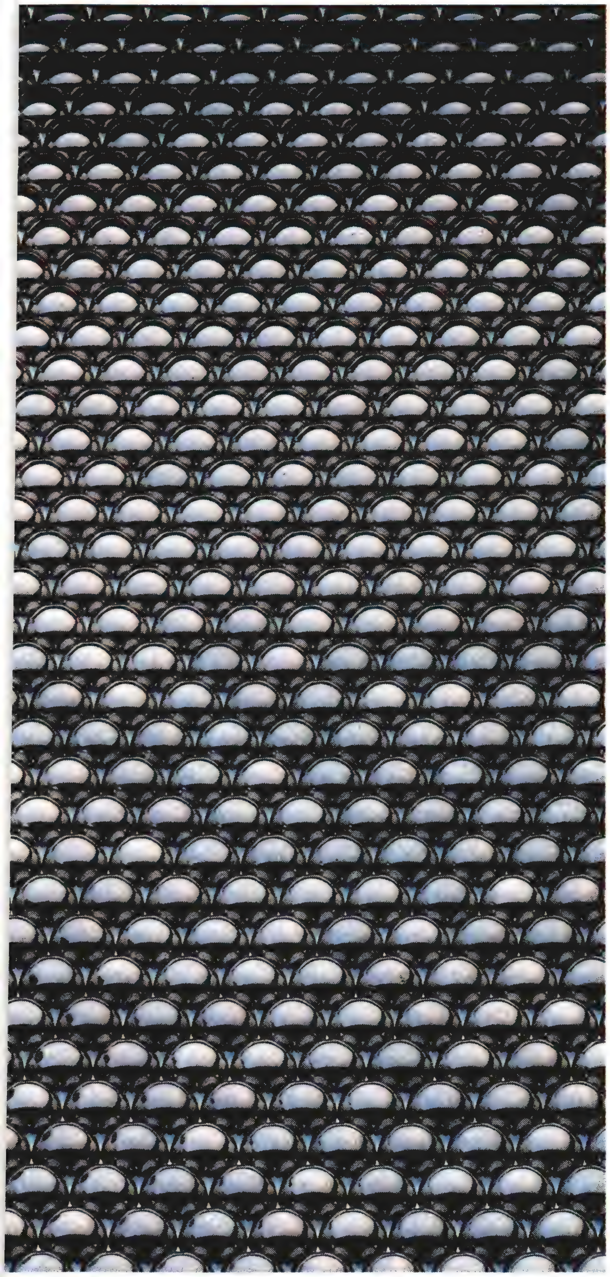

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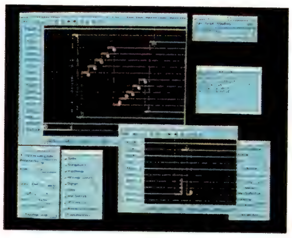

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CIRCLE NO. 112

New philosophy aids shift from schematic-based to HDL-based design

Charles F Shelor, Shelor Engineering

Using HDL-based techniques for developing hardware is similar to using high-level languages to develop software: An object-oriented design philosophy is directly applicable.

The critical path in a hardware-development schedule often involves the development of an ASIC—a gate array, a standard-cell array, a "compiled" silicon device, or programmable ICs, such as a field-programmable gate array (FPGA) or a complex PLD (CPLD). An ASIC that isn't ready on time or that fails to operate in a system (even after passing all of its test vectors) can delay a project by months. You can improve your productivity as an ASIC designer by using a hardware-description language (HDL) and logic synthesis, but HDL requires a new design philosophy to be most effective. A successful transition from schematic- to HDL-based design involves facing a number of different issues.

The transition to HDL-based design isn't difficult, but it does require some planning to avoid unexpected complications. Development of electronic hardware using HDL design techniques is similar to development of software projects using a high-level language. In particular, an object-oriented design philosophy is directly applicable, especially when using VHSIC (very-high-speed integrated circuits) Hardware-Description Language (VHDL).

To make a conscious transition from schematic- to HDL-based design, you must first be fully cognizant of details in the schematic-design process. A schematic doesn't just show how electronic components connect; it also provides information that helps you understand how a circuit operates. This information consists of component functionality, data dependencies or data flow within the circuit, feedback paths, locality of signals, and parallel vs sequential operation. Looking at **Fig 1**, digital circuit designers will immediately recognize U1 as an AND gate, U2 and U4 as rising-edge-triggered D flip-flops, and U3 as an exclusive-OR gate. **Fig 1a** shows Mil-STD-806C and ANSI-STD Y32.14 1 standard logic symbols. **Fig 1b** shows ANSI/IEEE-STD-91-1984 2 logic symbols.

As component complexity increases, representing functionality with visual graphics becomes more difficult. **Fig 2**'s symbols illustrate how complex symbology can get with MSI components. With LSI and VLSI components, symbols indicate only input or output, active-high or -low operation, level- or edge-sensitive triggering, and the type of drivers used for outputs.

Schematics and implicit information

Most good circuit designers provide a lot of implicit information on a schematic. Information flow, for example, normally goes from left to right. Vertical alignment typically represents operations that occur concurrently, although it may also represent independent operations. Many pipelined designs indicate stage synchronization by vertical alignment. Inputs normally appear on the left side of a schematic, and outputs appear on the right. Feedback paths appear as prominent signals that loop from right to left. Short signal lines connect only a few components; longer lines with many connections indicate a signal with greater scope. A special flag symbol indicates that a signal is nonlocal and provides a reference to the page or schematic coordinate of additional signal segments.

Rarely do schematics have attached notes that state any assumptions about the presentation of information. Someone looking at a schematic expects to get a lot of information in an implicit context from a style that designers have adopted via tradition.

Unfortunately, a textual source listing of HDL code doesn't provide all the information contained in a schematic's graphics. Although some of the graphical information is available—you have to provide names of interface signals and the directions of signal flows when you define VHDL components—other information doesn't easily fit into the HDL process. Signal feedback, locality, and sequenced vs parallel operation, for example, have no explicit graphical representation in HDL code. The HDL-development process must recognize these deficiencies and provide a means of compensation. When experienced circuit designers are just becoming familiar with HDL-based design, they often express a feeling of discomfort with the process. However, after being shown methods that compensate for information loss, they realize that information loss was the source of their discomfort.

The fact that missing information is indeed a problem is evident in the popularity of graphical tools as front ends to HDL design. Using graphics to show interactions among blocks or subcomponents of an HDL design is a popular approach. Several tools support transitions between graphical and HDL implementations; other tools translate state diagrams, spreadsheet-style Boolean tables, and other graphical representations to HDL implementations.

Methodology overcomes information loss

You can reduce or eliminate some of the problems that result from information loss by combining features of HDL with a consistently applied methodology. For example, recognition of a signal as input, output, or bidirectional is explicit in VHDL in the port *mode* declaration, so a naming convention for port signals can provide distinguishing information. For instance, "sname_c" can express a signal name (sname) and a code (c) that represents signal characteristics. A convention for the code could be

- b—active-high bidirectional
- c—active-low bidirectional
- f—falling-edge input
- i—active-high input
- j—active-low input
- n—active-low output
- o—active-high output
- r—rising-edge input.

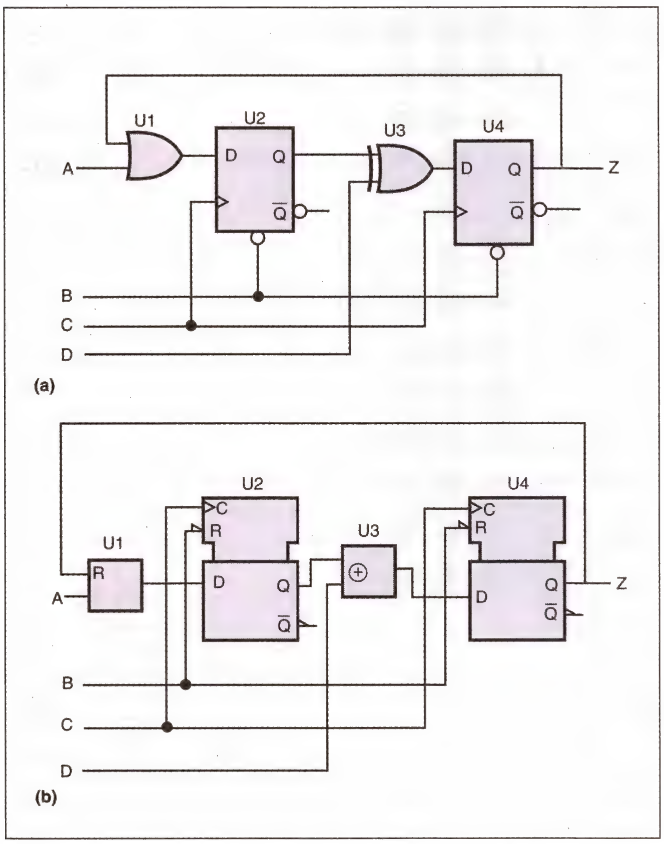


Fig 1—A schematic provides much more information than just showing how things connect. Graphic symbols—shown here in military (a) and ANSI (b) forms—show, among other things, component functionality. You can lose useful information such as this in HDL-based design unless you take precautions.

Comment statements in an HDL listing can supply other missing information. For example, a short comment on each signal can indicate the signal's purpose and its intended source or destination(s). You should also document feedback paths with comments. In some cases, the use of good comments actually overcomes some schematic shortcomings. With comments, you can explain why you selected a particular design approach, something that a schematic doesn't easily allow. Likewise, you can list other design approaches and explain why you rejected them.

HDL-based design can also free you from some unnecessary details. In schematic-based design, you work with available components in design libraries; even with ASICs and FPGAs, there is an underlying library of cells or macros. The HDL hides this library, freeing you from the details of clock-enabled flip-flops, active-high or -low presets or clears, and the number of inputs available for various gate functions. Your logic-synthesis tool accounts for these details much as a high-level-language compiler generates appropriate addressing modes in machine language from high-level source-program input.

The freedom from these structural details, however, does increase your responsibilities in some ways. For example, you must remember to provide for initialization of your implementations without the obvious reminder of an unconnected reset pin "dangling" on a schematic. You must also determine which signals should be stored and which signals are combinatorial. You must describe an interface in sufficient detail to distinguish correct and incorrect usage. These problems are not normally evident in small designs; they appear in the integration stages of large designs.

Get it right the first time

Two major productivity factors apply to large designs. For initial developments, getting the design right the first time is the most important factor, and the costly mistakes are those that impact interfaces. You can't discover an error until you integrate the components that use that interface. Then, when you make the design changes required to fix the error, you invalidate earlier tests, requiring their repetition. You might even need another pass of silicon for the ASIC, with a tremendous impact on cost and schedule.

For subsequent derivative developments, the most important productivity factor is reuse of prior effort. Every reuse of a tested component from a prior design reduces the cost, schedule, and risk of a current effort. This factor applies equally for schematic- and HDL-based designs. The reuse of bigger components provides larger reductions in schedule, cost, and risk. One of the main reasons for using HDL and logic synthesis in development is to generate larger ASICs. Therefore, most designers making the transition from schematic- to HDL-based design are also generating larger

ASICs. The opportunities for the reuse of larger components increase with larger ASICS.

The key to getting a large design right the first time is verification of results for each step, or phase, of development. In software development, the increased complexity of products has led to increased formalism and documentation of these phases, an approach that hardware engineers would do well to consider for designs with increasingly large gate counts.

Typically, the phases of a development process are requirements analysis (or definition), design, implementation, test, and integration. In a hierarchical development, each of these phases applies to each level of the hierarchy. Software engineers formalize the hierarchy levels as units, components, and configuration items. Units, the lowest level of the hierarchy, get implemented directly in the source code. To implement components, which represent one or more intermediate levels of hierarchy, software engineers integrate collections of units to obtain higher levels of capability. The top-level hierarchy, called a configuration item, results from assembling components into a complete software product.

Each of these levels of software development has a set of documentation that includes requirements, design, implementation, test, and integration. The configuration-item documentation for contracted efforts is usually a deliverable product that is contractually controlled. Often, government projects also require the delivery and control of component-level documentation. In hardware development, however, many customers of commercial development efforts consider documentation complete if they get a released schematic drawing. Even government contracts rarely require more than configuration-item documentation for hardware. Successful, well-organized, HDL-based designs should use a simple, inexpensive method of documenting requirements and design at the component hierarchy.

Some commonly recognized steps of a typical development process are:

- the generation of a schematic (considered to be design)
- fabrication of a circuit board (implementation)

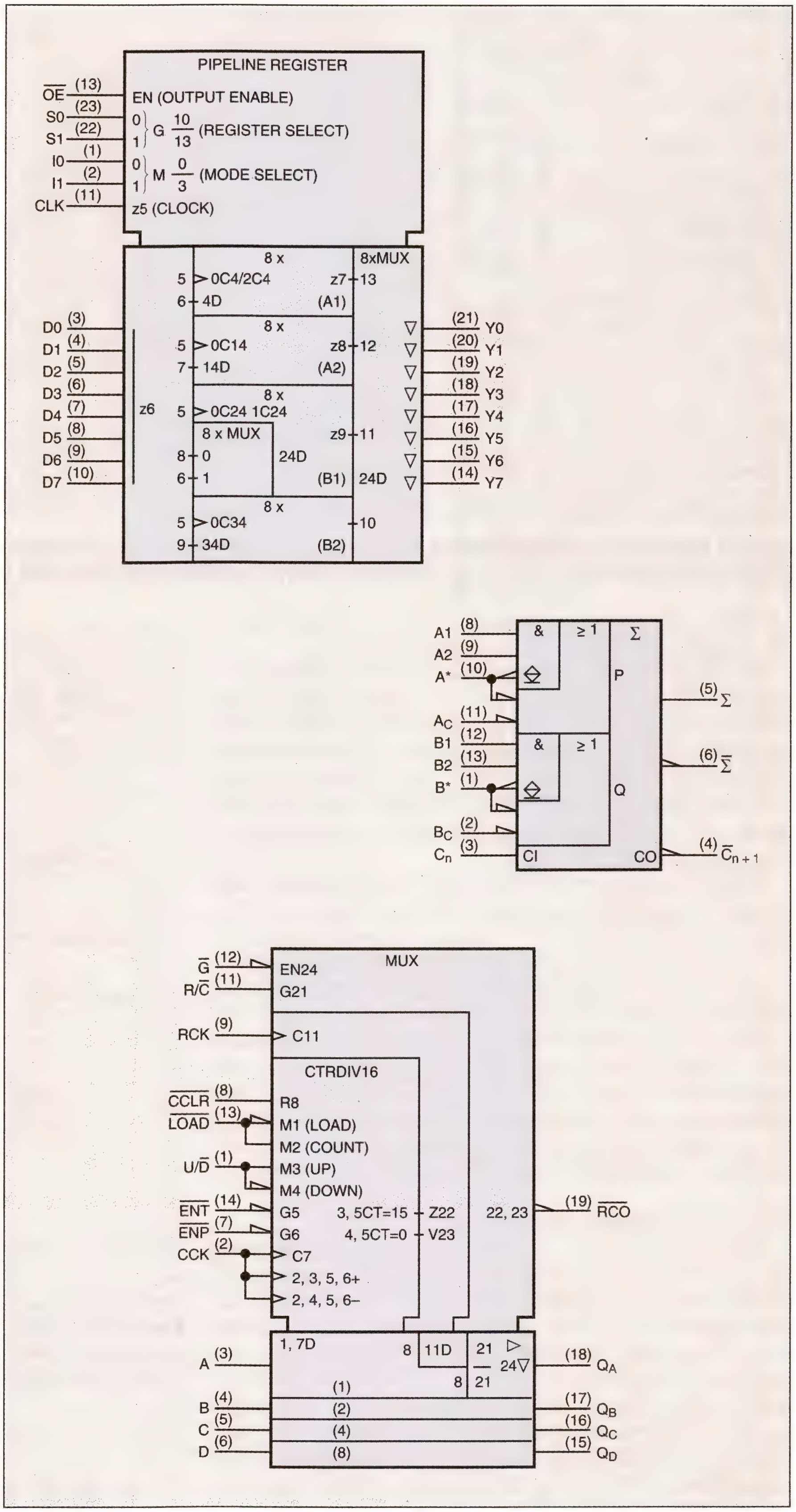
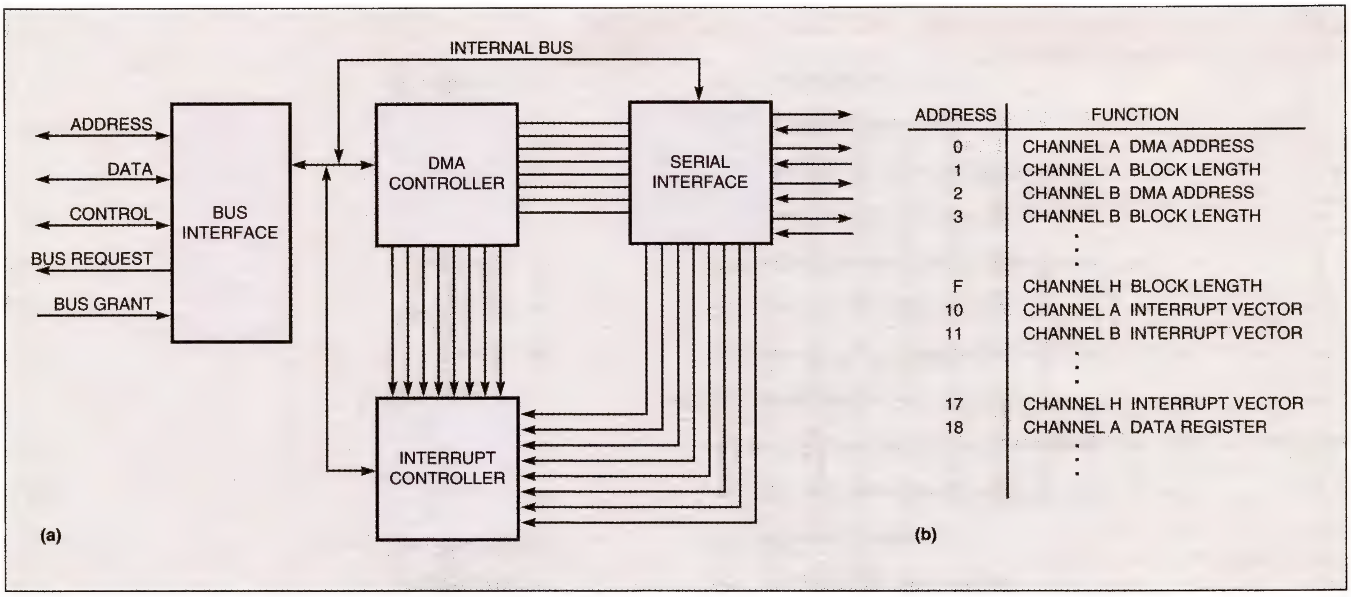


Fig 2—As component complexity increases, schematics become less effective at representing functionality. They are object-oriented in that they hide low-level detail.



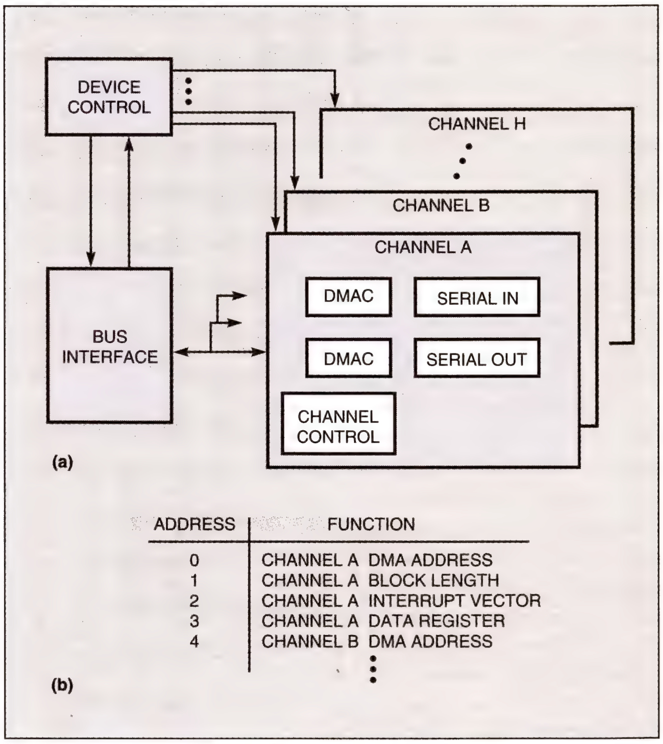
ADDRESS	FUNCTION
0	CHANNEL A DMA ADDRESS
1	CHANNEL A BLOCK LENGTH
2	CHANNEL B DMA ADDRESS
3	CHANNEL B BLOCK LENGTH
	⋮
F	CHANNEL H BLOCK LENGTH
10	CHANNEL A INTERRUPT VECTOR
11	CHANNEL B INTERRUPT VECTOR
	⋮
17	CHANNEL H INTERRUPT VECTOR
18	CHANNEL A DATA REGISTER
	⋮

Fig 3—A design may seem object-oriented when it is not, as illustrated by this eight-channel serial interface with DMA. Although the functional blocks (a) seem like a good set of objects, the registers for different channels have addresses that are intermixed (b).

- making the board operational in the laboratory (test)
- plugging the board into a box (integration).

These steps do not constitute the lowest level of a development hierarchy, however. The design, implementation, test, and integration efforts of the lower hierarchy levels rarely get formalized. Design, for example, occurs when you partition boards and ASICs into smaller units and determine the interfaces among the units. Block diagrams represent these designs, and very large designs have multiple levels of block-diagram hierarchy.

Design implementation occurs when you produce the next lower level block diagram, when you draw schematics, or when you write HDL programs. Testing at the lowest level occurs via simulation of individual blocks or HDL code sections. Integration consists of reconstructing your block diagrams, using schematics or HDL code sections, and testing the connected blocks as larger units. After the completion of each level of integration, development continues with the next higher level of the hierarchy. Treating the block diagram as a formal design step in the development process is a concept that is initially awkward for many designers, but it is a key concept for successful top-down development of large designs.



ADDRESS	FUNCTION
0	CHANNEL A DMA ADDRESS
1	CHANNEL A BLOCK LENGTH
2	CHANNEL A INTERRUPT VECTOR
3	CHANNEL A DATA REGISTER
4	CHANNEL B DMA ADDRESS
	⋮

Fig 4—Object-oriented techniques make designs reusable. As shown here in (a), each interface channel comprises five smaller objects: two single-channel DMA controllers, serial input, serial output, and channel controller. Register addresses (b) are sequential for each channel.

Design reuse boosts productivity

The largest potential productivity gain comes from reusing design pieces. To reuse a design piece, you must be aware of what pieces exist, what functions they provide, what prerequisites they need, what limitations they have, and what testing they have undergone. An original design that requires a 19,200-baud asynchronous serial channel with 7 bits and odd parity would not be reusable for a design that needed a 38,400-baud asynchronous channel with 8 bits and no parity. However, if the first design implemented an asynchronous serial interface with programmable bit length, parity, and baud rate, the first design would be directly reusable by the second design.

Schematic-based development doesn't guarantee reusability, however, even when you build in provisions for reuse. Incompatible library elements can result from changing ASIC vendors or even a technology change from the same vendor. With HDL-based design and logic synthesis, however, dependence on vendor and technology implementation practically disappears from a design. The

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situation is analogous to the use of a high-level language for software development. In fact, HDL-based hardware development is so similar to software development that the dominant HDLs are based on successful software languages such as C, Pascal, and Ada. Logic-synthesis tools accept the HDL definition and generate gate-level implementations, much like a computer-language compiler produces machine instructions from source code.

Like structured programming in the 1970s and early 1980s, HDL-based design has been accompanied by top-down design with limited success. But, like structured programming, top-down design isn't necessarily bad, just insufficient by itself. In software development, object-oriented development provides some important missing details.

With schematic-based hardware development, designers have been constrained to producing object-oriented designs. Schematics, after all, are composed of an interconnection of library component objects. The advent of ASICs and HDL-based logic synthesis, however, allows the hardware engineer to escape the bounds of object-based development and get mired in the swamp of unstructured implementations.

Object vs function

Often, the distinction between an object-oriented design and a functionally oriented design is subtle. Consider, for example, an eight-channel, multiple-protocol serial interface with DMA. A possible first-level design of the device (**Fig 3a**) places all of the DMA logic in a block, all of the serial logic in a block, and all of the interrupt control in a block. When labeled as DMA controller, serial interface, and interrupt controller these blocks seem like a good set of objects. They seem reusable any time you need an eight-channel DMA controller. The original purpose, however, was not to build a universal DMA controller, but to build eight channels of serial interface. The software interface for the new design would be awkward, because the various registers for the channels would have addresses that are intermixed (**Fig 3b**).

A better organization for the registers, shown in **Fig 4**, allows the software to encapsulate the serial-interface control into a single Ada record, a C structure, or a C++ object. (The implementation of this design could also encapsulate the interface control into a VHDL record.) Each interface channel comprises five smaller objects: two single-channel DMA controllers, serial input, serial output, and channel controller. Reuse of components can be applied at several levels, making the generation of a 6- or 11-channel device much easier than using the original design.

Another advantage of this partitioning is the reduction in global wiring for interconnecting blocks. The interconnection and routing of long signals in ASICs can consume a large amount of silicon and time. Minimizing global interconnect or top-level wiring results in smaller, faster devices, corresponding to the software guidelines of maximum cohesion and minimum coupling. A quick metric for partitioning evaluation is the sum of the ports at a hierarchy multiplied by the hierarchy's distance from the bottom. Larger values for this number represent more difficult routing of the design. This partitioning also reduces the possibilities of inadvertent interactions among the channels.

You should apply the principles of object-oriented design at each level of the hierarchy, such that the final object, the ASIC, is composed of smaller objects. Each of the smaller objects, in turn, is composed of even smaller objects, continuing until each object is small enough for easy implementation as an HDL unit such as a VHDL entity. The resulting structure is easier to implement, test, and integrate, and it provides objects that are reusable in future projects. EDN

Author's biography

Charles Shelor is head of Shelor Engineering, a consulting company in Arlington, TX. In addition to training schematic-capture pc-board designers in using VHDL logic synthesis for ASIC and FPGA designs, Shelor develops VHDL models and performs beta tests and evaluations of VHDL products. He has BSEE and MSEE degrees from Louisiana Tech University and is pursuing a PhD in computer science engineering at the University of Texas at Arlington.

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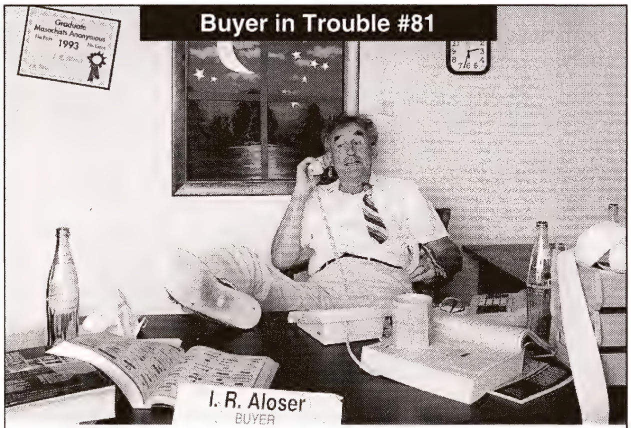

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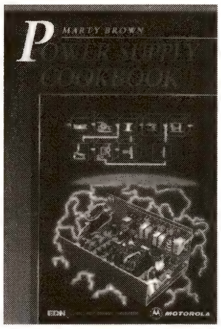

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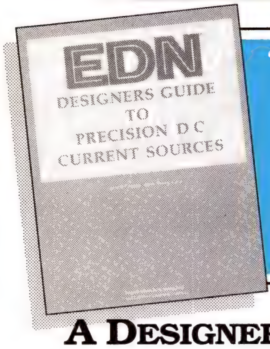

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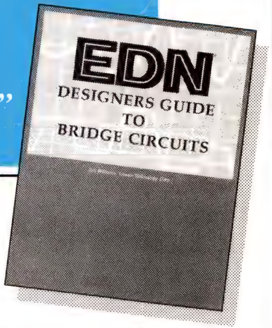

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Key-embedded joystick controls cursor and Windows functions

J-Mouse III technology enables a keyboard's J key to function either as a normal J key or as a joystick.

In a computer keyboard that incorporates a new technology known as "J-Mouse III," the J key packs a lot of punch. When you type, the J key functions like any J key, but when you hold the key down, it becomes a cursor-controlling joystick. Holding the J key down also adds capabilities to other keys, turning them into so-called Wizard keys. Wizard keys can emulate mouse buttons or activate common Windows functions, such as cut, copy, and paste. And, unlike other pointing-device technologies, J-Mouse III requires no space other than the J key that a keyboard must have anyway.

When you depress the J key in a system that incorporates J-Mouse III, the system automatically distinguishes text entry from cursor control or Wizard-key activation. When you type text, you depress keys very briefly; when you use the J key for another purpose, you hold it down longer. By noting how long the J key remains activated, the system determines your intended use of the key.

The J key in a keyboard that incorporates J-Mouse III technology has a spherical depression in its surface. The depression isn't noticeable when you type, but it's useful when you use the key as a joystick. With your index finger, you apply slight pressure in the direction of intended cursor travel. Force-sensing resistors (FSRs) convert pressure to cursor motion. Although some early applications of FSRs produced somewhat jerky cursor motion, a patented spring mechanism in the J key of J-Mouse III systems supposedly eliminates that problem.

The J-Mouse III technology is available by licensing and is most applicable for high-volume keyboard production. In such applications, implementations will cost "a few dollars," according to the developer.

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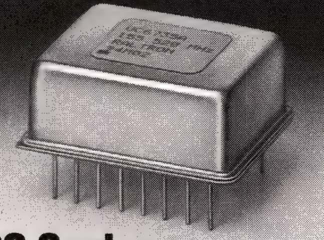

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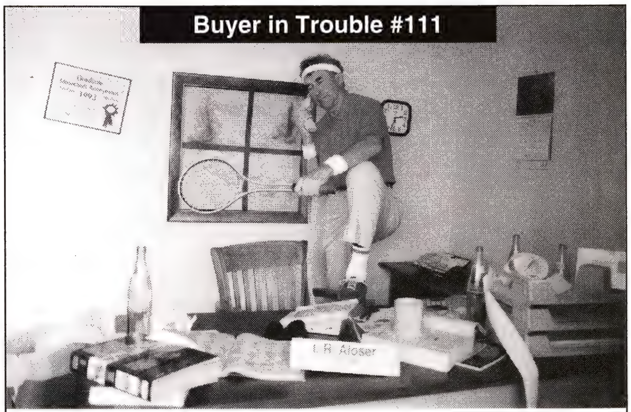

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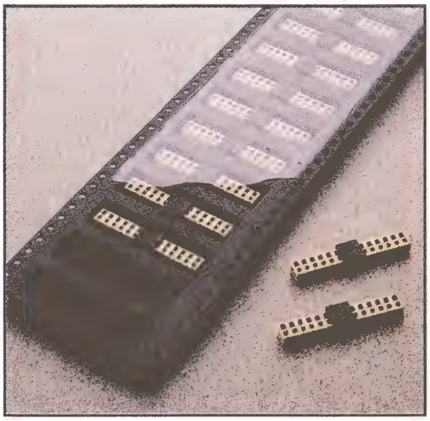

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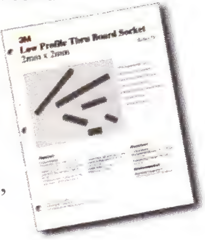

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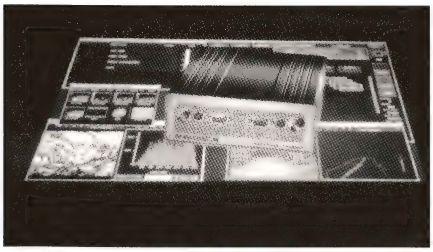
CIRCLE NO. 26

rates to 10 Mbytes/sec. A utility called "AutoSCSI" allows easy installation and configuration. All the cards are available with floppy-disk support, and the EISA and VESA versions are also available without it for $20 less. Prices without floppy support are $449 (EISA) and $279 (VESA and ISA). **Bus-Logic Inc**, Santa Clara, CA. (408) 492-9090. **Circle No. 360**



Video processor has SCSI interface. The DASM-VIP video-image processor combines a 24-bit frame grabber and a DSP-based image processor in a unit that connects to virtually any computer via a SCSI connection. For simplicity of use in accessing image data, the unit emulates a SCSI disk drive. A 33-MFLOPS TMS320C31 DSP is the system processor; real-time video input can come from RGB, NTSC, and S-Video color sources and from RS-170 monochrome sources. Digital sync-lock circuitry virtually eliminates pixel jitter and assures precision image data from noisy video sources, including VCRs. $2995. **Analogic Corp**, Peabody, MA. (508) 977-3000, ext 3441. **Circle No. 361**

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PCMCIA card provides serial port. A new Type II PCMCIA card provides a serial interface for portable computers. The card includes an internally buffered 16550 UART and an 8530 USART for asynchronous or synchronous communication. You can configure the asynchronous port as COM 1, 2, 3, or 4. The synchronous port is fully programmable. $145 (100). **Smart Modular Technologies**, Fremont, CA. (510) 623-1231, ext 104. **Circle No. 363**

Kit enables keyboard evaluation. An evaluation kit lets you check out the FKB7316 membrane-technology keyboard for your laptop- and notebook-computer OEM applications. The kit includes a keyboard, an evaluator board, cabling, connectors, and documentation. The evaluator board has a keyboard controller/encoder IC that enables connection of the keyboard to an IBM-compatible keyboard port. $100. **Fujitsu Microelectronics Inc**, San Jose, CA. (800) 642-7616. **Circle No. 364**

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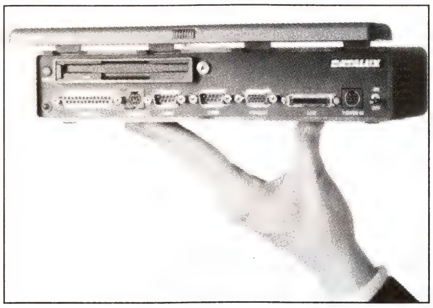

PC is built like a brick. The Databrick is a transportable PC the size and shape of a brick (26×12×5 cm). It has no display, keyboard, battery, or accessible bus slots; it's intended for applications where these features are unnecessary. The PC includes a 486 μP, up to 32 Mbytes of memory, floppy- and hard-drive controllers, two serial ports, a parallel port, a keyboard port, and a local-bus VGA port. Other options are also available. $800 (1). **Datalux Corp**, Winchester, VA. (703) 662-1500. **Circle No. 366**

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Fast, flat computer has high-resolution color display. The flat-panel DisplayPac-SVGA computer has an 11.8-in. active-matrix color TFT LCD that provides a 1024×768-pixel, 64,000-color display. The processor is a 486DX4 that operates at clock rates to 100 MHz. Main-memory capacity is 32 Mbytes. PC features and options for the 14.5×10.5×3.5-in. unit include floppy- and hard-disk drives, a 1.5-Mbyte semiconductor disk, a PCMCIA drive, and a resistive touchscreen. System expansion is possible via as many as six PC-bus slots. From $9861 (OEM). **Computer Dynamics Inc**, Greer, SC. (803) 877-8700. **Circle No. 367**

Disk drives serve audio/video applications. Two disk drives—the 5.25-in. Scorpio Model 1991AV and the 3.5-in. Taurus Model 4110AV—provide the high sustained transfer rates necessary in audio and video applications to prevent frame dropouts and jerkiness in audio or video output. The Scorpio has a sustained rate of 6.4 Mbytes/sec; the 1-in.-high Taurus' rate is 4.3 Mbytes/sec. Capacities are 9.1 and 1 Gbytes, respectively. Suggested list prices are $5455 and $1255, respectively. **Micropolis Corp**, Chatsworth, CA. (800) 395-3748. **Circle No. 368**

Filter converts tiny monochrome CRT to color. RGB Fast Filter is a small, electrically switchable RGB color filter that allows you to display full-color images on a small (approximately 1-in.), high-resolution, monochrome CRT. Typical applications are head- and helmet-mounted displays. The filter has selectable red, green, and blue states that are switchable in 100 μsec. By displaying color fields at three times the normal 60-Hz video rate and by simultaneously switching the filter's color states, the system can "fool" your eyes into seeing blended, continuous color. Because monochrome CRTs can have high resolutions, the result is a compact and higher resolution color display than would be possible with a color CRT or LCD. $995 (1); potentially much cheaper in very large quantities. **Displaytech Inc**, Boulder, CO. (303) 449-8933. **Circle No. 369**

Laptop computer meets mil specs. The RMC-4000 rugged mobile computer meets MIL-STD-461/462 for EMI and RFI and MIL-STD-810E for shock, vibration, humidity, salt fog, dust, rain, atmospheric pressure, and temperature. The 9.6-lb, 486-based computer includes a 64-shade, monochrome VGA display and a flat-panel mouse. Faster processors and a color display are options. The system includes a range of I/O ports, plus optional PCMCIA slots and disk drives. $5995. **US Microtel Inc**, Richardson, TX. (214) 994-9078. **Circle No. 370**

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03702-022-13112	1x12	13mm	7.20″	2.40″	0.90″
03702-024-09116	1x16	9mm	6.70″	2.30″	0.90″
03702-026-09120	1x20	9mm	8.30″	2.35″	0.95″
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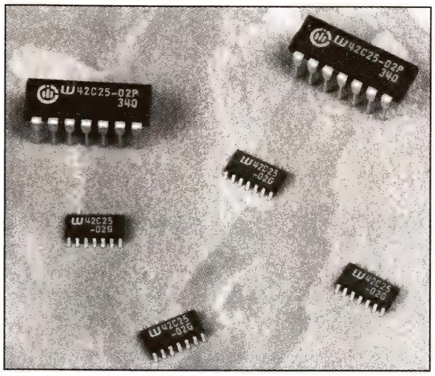

Pentium clock generator provides triple output. The W42C25 is a single-VCO clock generator with three output signals. The device uses a PLL with a crystal or reference clock to produce a low- phase-jitter duplicate of the source clock, a CPU clock, and a 2×CPU-clock signal. The two synthesized clocks come from a selection of eight preprogrammed frequencies stored in ROM and can switch between frequencies without output-signal glitches. The output signals vary from 2 to 120 MHz. The device draws 10 mA at 5V and comes in a 14-pin DIP or SOIC. Cost is $1.80 (1000). **IC Works Inc**, San Jose, CA. (408) 922-0202. **Circle No. 396**

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CPLDs have 128 macrocells. The CY7C374 and CY7C375 are 128-macrocell versions of the company's FLASH family of complex programmable-logic devices (CPLDs). The CPLDs employ 0.65-micron technology and have 100% routable interconnects. The CY7C374 has 64 I/O pins and comes in an 84-pin PLCC and a 100-pin TQFP. The CY7C375 has 128 I/O pins in a 160-pin TQFP The CY7C374 in a PLCC costs $31.45 (100). **Cypress Semiconductor Corp**, San Jose, CA. (408) 943-2600. **Circle No. 397**

Fully integrated read-channel IC runs at 80 Mbps. The 5V MC34245 peak-detect IC is pin- and software-compatible with the company's 3V MC34244 hard-disk-drive IC. The MC34245 provides the functions for the read-write channel of a constant-density hard-disk drive, including AGC, active filter, pulse detector, data synchronizer, frequency synthesize, servo demodulator, RLL1, 7 encoder/decoder, and power management. The device comes in a 64-pin TQFP; price is $16.50 (10,000). **Motorola Inc**, Tempe, AZ. (602) 897-5353. **Circle No. 398**

RF power amplifier operates from 3V battery. The ITT332101BD produces 1W of RF power output when driven with a 1-mW signal—a 30-dB power gain—while operating from a 3V battery. The GaAs IC suits cellular-radio power applications in the 824- to 849-MHz frequency band. The IC operates in the compressed Class A mode, which increases efficiency. In 16-pin SOICs, the IC costs $9 (10,000). **ITT Gallium Arsenide Technology Center**, Roanoke, VA. (703) 563-8600. **Circle No. 399**

Power-factor controller has precise overvoltage protection. The L6560 limits overvoltages to 5% and increases power factor to around 99%. The controller IC operates in transition mode and has a totem-pole output stage

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that drives power MOSFETs and insulated-gate bipolar transistors with source and sink currents as high as 400 mA. The IC also integrates a start-up timer, a temperature-compensated bandgap reference, and an undervoltage lockout with hysteresis that allows starting on currents as low as 0.5 mA. Quiescent current is <3.5 mA. In 8-pin DIPs and SOICs, the IC costs <$1 in OEM quantities. **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 400**

PCMCIA controller handles mixed voltages. An upgrade path for PCMCIA systems, the VG-469 controller works with various interface voltages. It offers two sense pins for detecting card voltages and hardware to prevent damage to low-voltage cards inserted into a 5V-only system. It controls two cards with independent operating voltages. The device is compatible with the PCMCIA 2.1 ExCA extension, Microsoft Plug and Play, and PC-card DMA operation. It supports memory and I/O cards, ATA hard-disk drives, and solid-state disks and offers the B-step register set. Price is <$15. **Vadem**, San Jose, CA. (408) 943-9310. **Circle No. 401**

Single chip integrates RAM and ROM. The LH6P81T combines RAM and ROM on a single chip. The device allows you to program fixed data into ROM of arbitrary size within the RAM area at the time of order placement. Features include 0.6-μm process, 512k×16-bit configuration, 80-nsec access time in normal mode, 40-nsec access time in page mode, 3.3V supply, and maximum current draw of 40 mA when active and 30 μA in standby. $48 (100). **Sharp Electronics Corp**, Camas, WA. (800) 642-0261. **Circle No. 402**

Communications processor allows program control. The VPS10101 communications processor, called the Ruby chip, is an ARM processor coupled with a UART, synchronous serial I/O, and parallel I/O to handle communications. The device offers a PCMCIA and an ISA host interface, operates over a 2.7 to 5V range, and has several power-management modes. Software-development tools for the device include C compilers, assemblers, simulators, and a development card for Unix and PC systems. The device costs $31.90 (10,000). **VLSI Technology Inc**, San Jose, CA. (408) 434-7995. **Circle No. 403**

Second-generation Saturn ATM interfaces appear. The PM5346 and PM7345 physical-layer interface ICs for asynchronous-transfer mode (ATM) are second-generation devices. The PM5346 and 345 offer link-level flow control and E3 framing, respectively. The PM5346 provides synchronous-optical-network and synchronous-digital-hierarchy framing, clock recovery,

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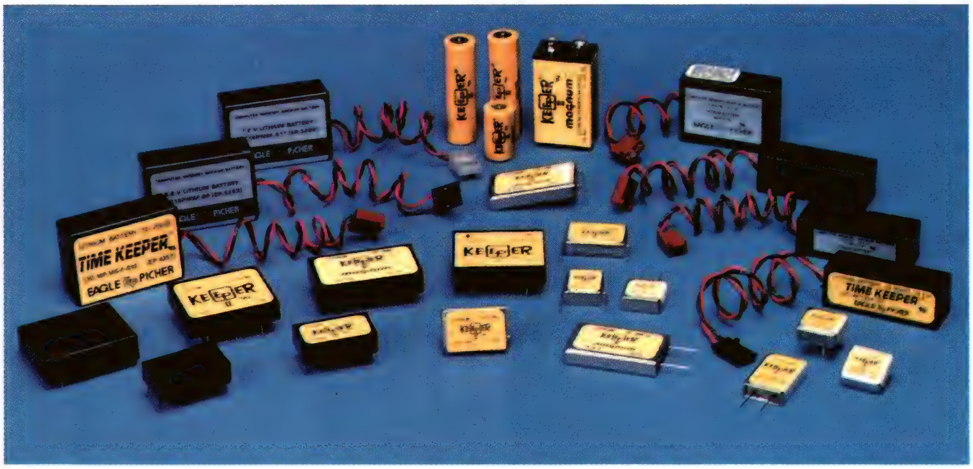

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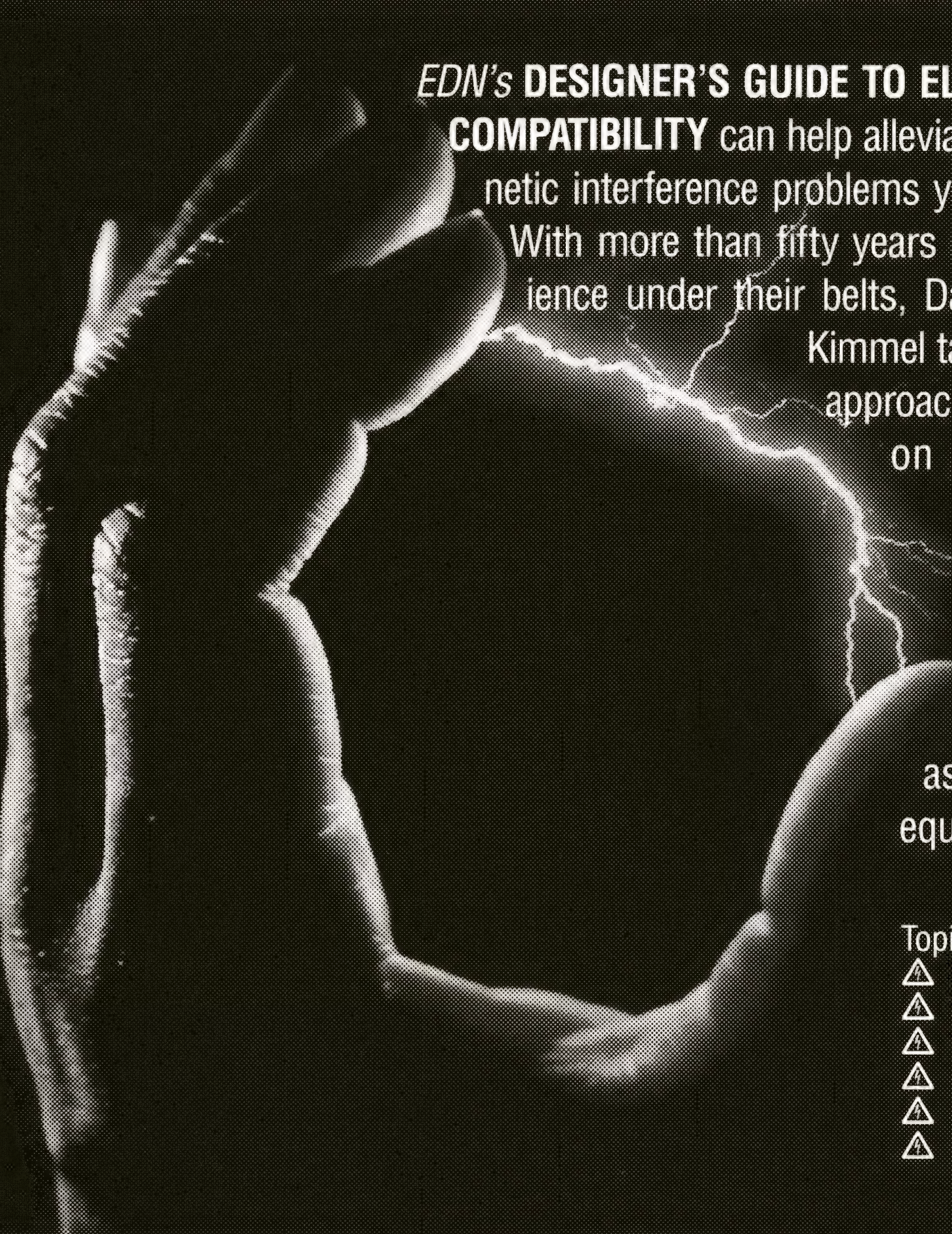

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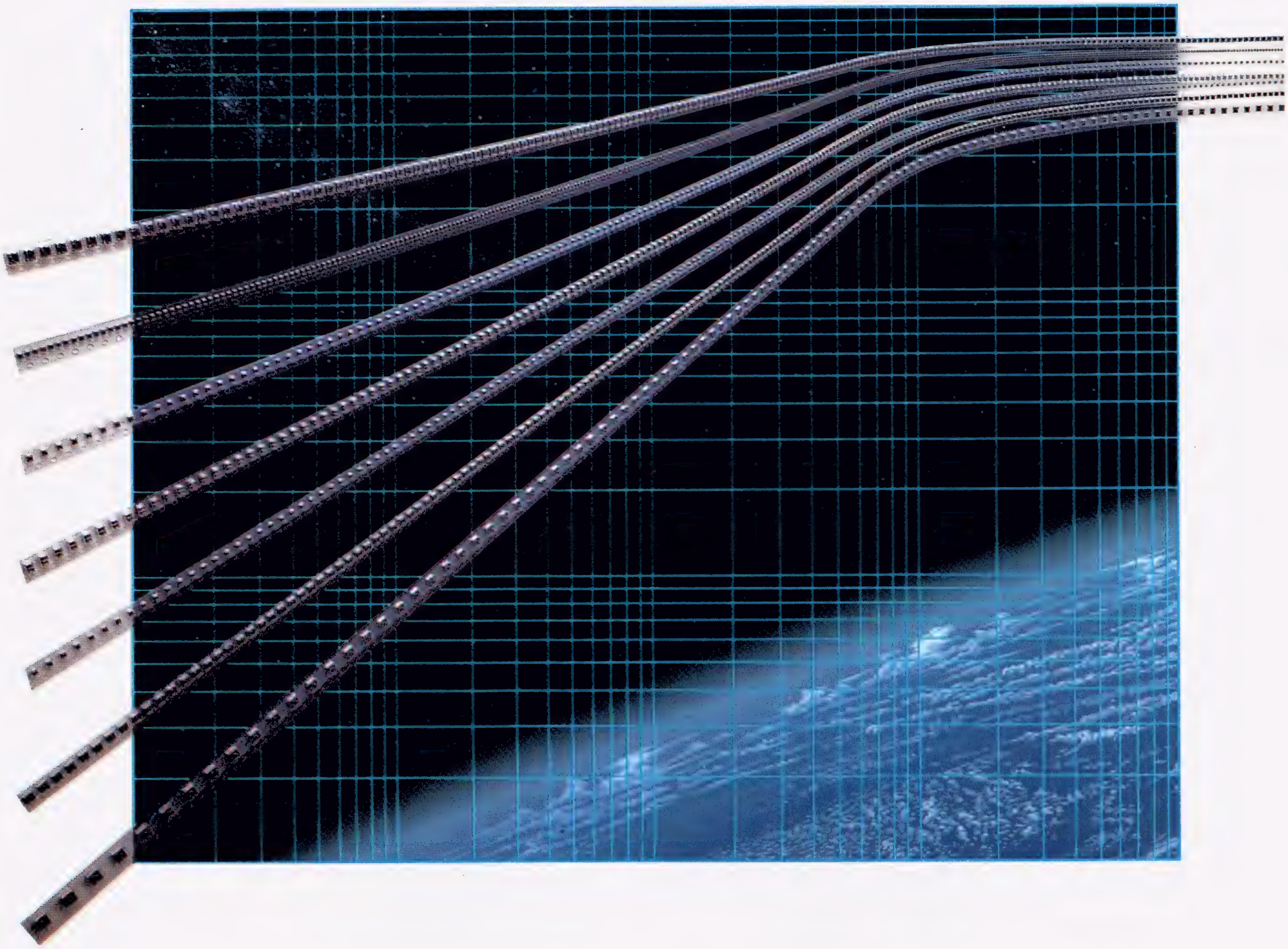

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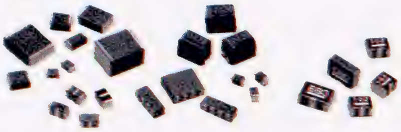

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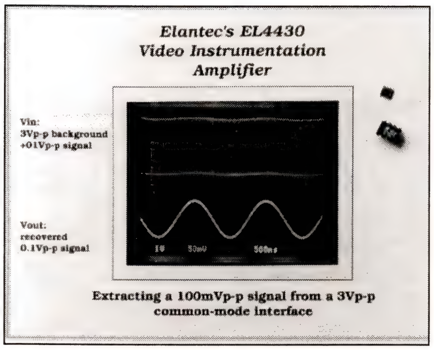
and clock synthesis at speeds to 155 Mbps. The PM7345 provides framing and interface to DS-1, DS-3, E1, and E3 telecommunications links operating at speeds to 45 Mbps. The PM5346 costs $68 (10,000); the PM7321, $75. **PMC-Sierra Inc**, Vancouver, BC, Canada. (604) 668-7348. **Circle No. 404**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Controller brings RDRAM to MIPs. The µPD31443 Rab^{2}it-BRAC chip combines a memory controller for the Rambus DRAM (RDRAM) with a bus interface to the 64-bit VR4200 or VR4400PC Mips processors. The devices work with processor clock speeds to 150 MHz at a bus rate of 40 MHz and RDRAM transfer rates of 500 Mbytes/sec. They feature a two-way read prefetch buffer and a two-entry write buffer, providing performance comparable to that of secondary caches. Samples will be available by the third quarter at a price of $100. **NEC Electronics Inc**, Mountain View, CA. (415) 965-6159. **Circle No. 406**

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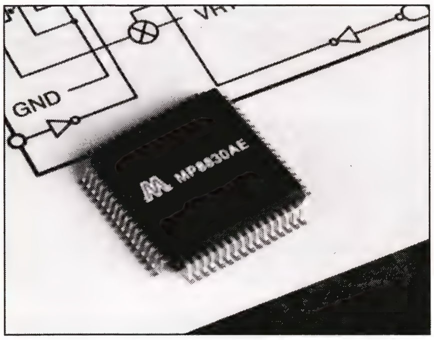
SBus, the MC92005 needs no additional glue logic. The slave devices, along with a configuration EPROM, connect to a programmable peripheral bus (PBus). The PBus includes arbitration logic, allowing bus masters, such as DMA controllers, on the local bus. The device works over the SBus speed range of 16.67 to 25 MHz and offers a peak bandwidth of 80 Mbytes/sec to the user. The 160-lead IC costs $30 (1000). Dawn VME Products (Fremont, CA) offers an evaluation board using the device. **Motorola Inc**, Chandler, AZ. (602) 814-4560. **Circle No. 407**

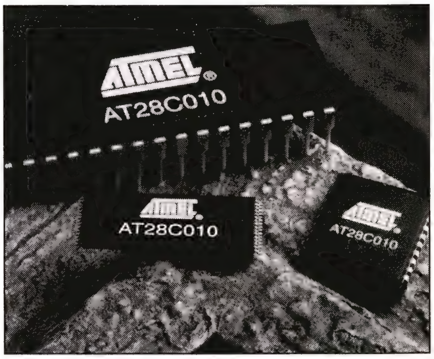


Triple ADC integrates gain and offset controls on all channels. The MP8830 color-imaging subsystem contains three independent, simultaneous-sampling ADCs, which provide pixel-to-pixel correction of CCDs and other inputs by updating gain and offset parameters from an external correction memory. 9- and 6-bit DACs drive each ADC's positive and negative reference voltages, respectively, to adjust each channel's gain and offset independently. The IC operates from a 5V supply and an external 1V reference and typically consumes 500 mW. The minimum sampling rate is 1.25M samples/sec. $33.33 (1000) in a 64-pin PQFP. **Micro Power Systems**, Santa Clara, CA. (408) 727-5350. **Circle No. 408**

Power controller meets PCMCIA 2.1 specs. The MIC2560 power-control matrix manages the main-supply and program voltages of PCMCIA slots. The IC replaces unprotected switching matrices or discrete ICs that can require six to 10 power MOSFETs and associated glue logic. The 2560 fits between a PCMCIA controller and a socket and requires no external components. Current-limiting and overtemperature shutdown protect all outputs from short circuits. In a 16-pin SOIC, the IC costs $2.96 (1000). **Micrel Semiconductor**, San Jose, CA. (408) 944-0800. **Circle No. 409**

Duplex Ethernet IC includes filters. The LXT907 universal 10BaseT adapter includes transmit and receive filters, a media-access unit, encoder/decoders, and physical-layer signaling circuits for connecting an Ethernet controller to an attachment-unit interface or to twisted-pair wiring. The device works in full-duplex switched Ethernet applications and costs $11 (1000). **Level One Communications Inc**, Folsom, CA. (916) 985-3512. **Circle No. 410**

Octal DAC has 13-bit resolution. A single MAX547 replaces eight DACs and eight precision op amps. The DAC is monotonic over the full operating-temperature range and requires no external components. You can configure its output for a variety of voltage swings in unipolar or bipolar mode. A high-speed double-buffered parallel port and 5-μsec settling allow fast updating, which the DACs can do independently or simultaneously. An asynchronous-clear input resets all eight outputs. The devices come in 44-pin flatpacks and PLCCs; prices start at $29.60 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 411**



1-Mbit EEPROM is in volume production. The AT28C010 1-Mbit EEPROM has a 128k×8-bit organization. The part has the same capabilities as those of a standard sealed military circuit but comes in a plastic package to reduce cost. The device has a read-access time of 120 nsec and a maximum page-write cycle time of 10 msec. Power-supply current draw is 80 mA in active mode and 300 μA in standby mode. The chip also employs JEDEC-standard software protection that prevents system noise from erasing data. The devices can typically write 1 byte or a full page of data in 7 msec. $50 (1000). **Atmel Corp**, San Jose, CA. (408) 441-0311. **Circle No. 412**

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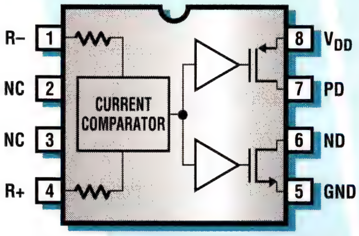
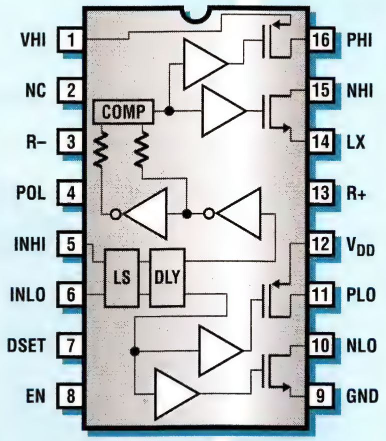
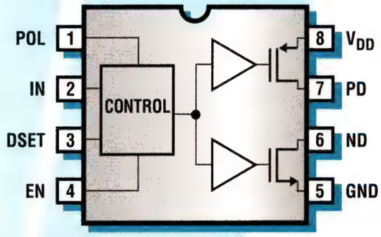


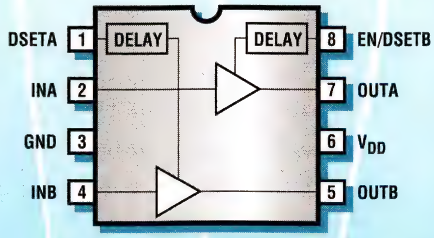
EL7761C
Half Bridge Driver



EL7861C
Single Delay Driver



EL7961C/7971C/7981C
EL7962C/7972C/7982C
Dual Delay Drivers



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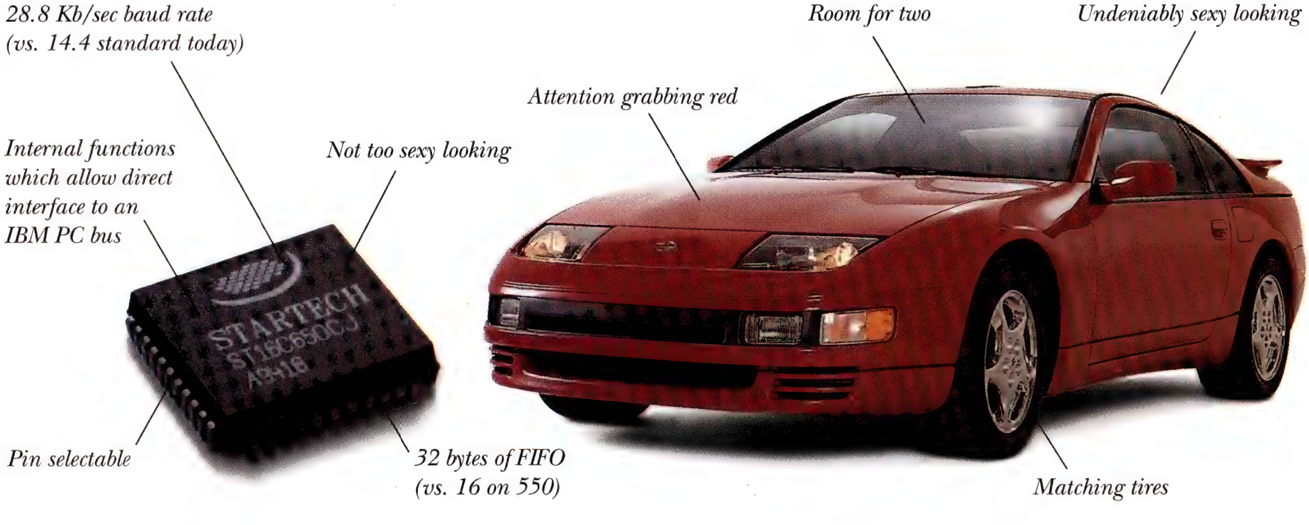
Both are turbos with a V6 engine, but the one on the left will launch the next generation of modem devices.



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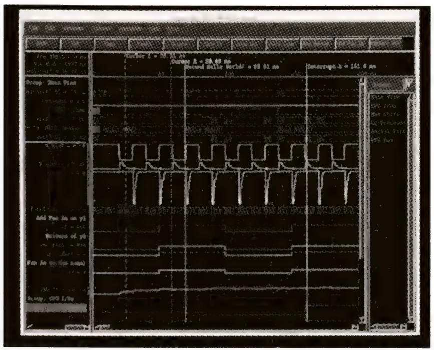
Explore state machine and datapath logic functions. Insight/sm for state machines extracts a design's state-machine definition and displays a state-transition table that shows reachable states, transitions, deadlock states from which the machine cannot advance, and transitions that do not depend on the current state. For datapath designs, Insight/dp generates a symbolic truth table from a list of data and control signals. The products will be available in September, and the two-product bundle will cost $9995. **Chrysalis**, Andover, MA. (508) 475-7700. **Circle No. 346**



Waveform viewing and analysis tool lets you view signals from mixed-simulation environments. Signalscan 3.0 lets you view integrated waveform displays from both analog and digital simulators. The initial product works with a variety of Verilog simulators plus some analog simulators. Analysis features include the ability to trace backwards from signals to drivers. Signalscan 3.0 costs $4995. **Design Acceleration Inc**, San Jose, CA. (408) 559-8500. **Circle No. 347**

Tool concurrently analyzes signal integrity, EMI, and thermal characteristics. Designers of pc boards and multichip modules must create layouts that satisfy the requirements for signal integrity, EMI, thermal characteristics, and reliability. Because the layout has such a significant effect on all the above characteristics, it's difficult to arrive at a satisfactory design while addressing each issue individually. Unisolve is a combination of five integrated tools that costs $115,000; alter-

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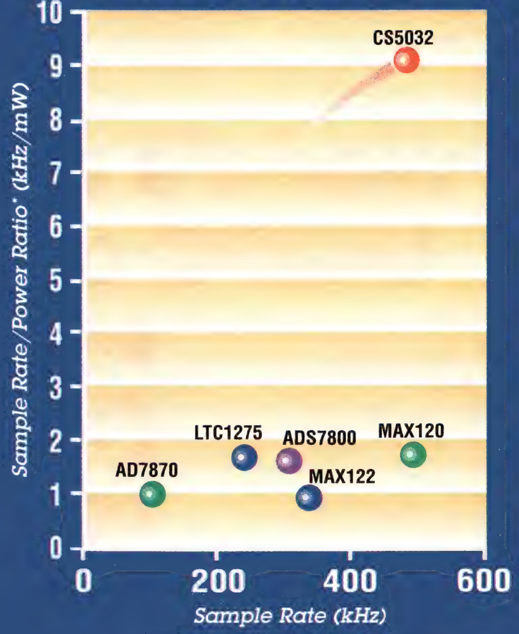

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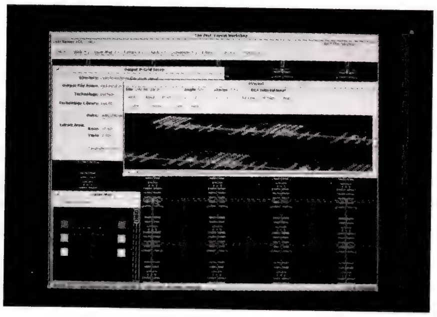
natively, you can purchase each tool separately. **Unicad**, Westford, MA. (508) 692-8446. **Circle No. 348**

Logic-emulation family targets ASIC and board-level emulation. Explorer ASIC emulates 30,000-gate ASICs at 10 MHz. Explorer MP3 lets you emulate board-level designs with much higher gate counts, depending on standard components you provide, such as multichip modules, µPs, microcontrollers, RAM, ROM, DSP, and field-programmable gate arrays. Prices for typical configurations, including hardware and software, range from $40,000 to $80,000. **Aptix Corp**, San Jose, CA. (408) 428-6200. **Circle No. 349**

Floor planner offers detailed placement capability. Floorplacer bridges the gap between front-end design and back-end layout. The tool works with the company's layout tools, letting you position embedded blocks within embedded arrays, including custom blocks. The tool analyzes embedded-array floor plans for routability and timing correctness. Floorplacer costs $25,000 and will be available in the third quarter. **Silvar-Lisco**, Mountain View, CA. (415) 962-3000. **Circle No. 350**



3D extraction and simulation tool for ICs offers accurate analysis. Solving fields in 3D, Net-An extracts accurate capacitance and resistance parasitics for Spice simulation of IC networks. P-Grid solves fields in 3D for extraction and simulation of resistance parasitics, voltage, and current densities for analyzing the power and ground networks on ICs. Net-An and P-Grid sell for $75,000 and will be available in September. **OEA International Inc**, Santa Clara, CA. (408) 738-5972. **Circle No. 351**

PLD tool adds Verilog synthesis. The Max+Plus II software now accepts Verilog HDL-based designs. You can also use the Verilog-entry capability for the company's 50,000-gate programmable multichip modules for ASIC prototyping. The Verilog-HDL entry option costs $2995 on PCs and $4995 on Unix workstations. **Altera Corp**, San Jose, CA. (408) 894-7110. **Circle No. 352**

Formal-proof verifier compares designs. The BoolesEye formal-proof verifier compares any register-transfer, gate-, and transistor-level description with another without test patterns to exercise the design. The tool is useful for verifying refinements to a design. The gate-level base package costs $30,000, and the transistor-level option costs $20,000. **Altium Inc**, San Jose, CA. (408) 534-4100. **Circle No. 353**

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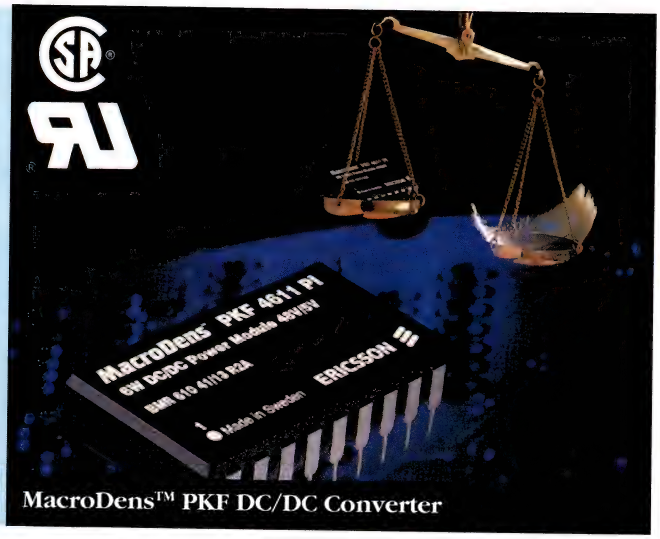

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256Kx32	EDI8F32257C*	17	64 pin ZIP
32Kx24	EDI8F2432C	15	56 pin ZIP
64Kx24	EDI8F2464C	15	56 pin ZIP
128Kx24	EDI8F24128C	20	60 pin ZIP

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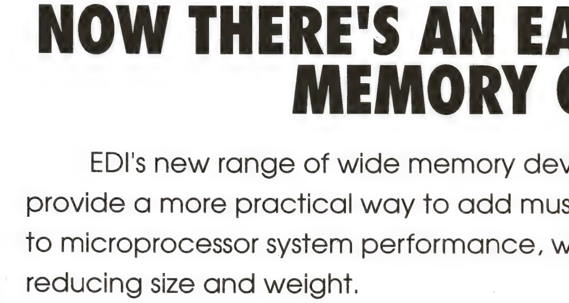

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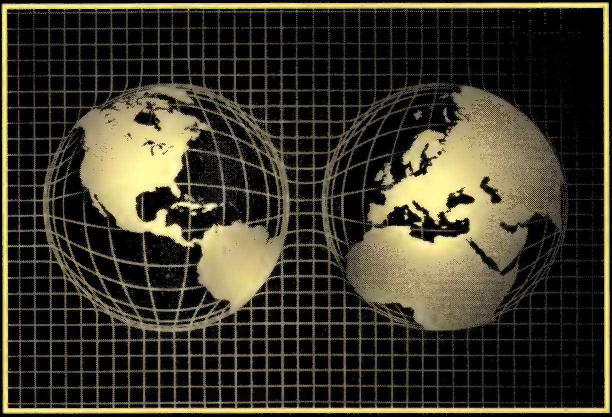

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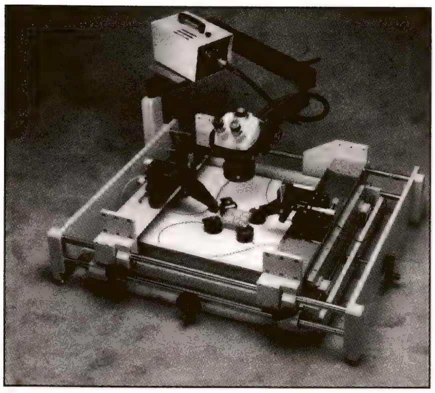

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OEM PC data-acquisition boards require no expansion slots. The 8×7-in. DaqBook/216/OEM (16-bit ADC, $1495) and -/112/OEM (12-bit ADC, $995) attach to DOS or Windows PCs in three ways: via a standard parallel port, a high-speed enhanced parallel port (EPP), or a PCMCIA interface. You can mount the units, which require 10 to 20V-dc power, in any location accessible to a cable for the type of interface you select. Each board offers eight differential or 16 single-ended analog inputs, two 12-bit analog outputs, four digital inputs, four digital outputs, and a counter/timer. Both models take 100k samples/sec, accept plug-in signal conditioners, and expand to 256 channels. **IOtech Inc**, Cleveland, OH. (216) 439-4091. **Circle No. 382**

VXIbus embedded controllers run at 100 MHz. The VXIpc-486 Model 599 uses a 100-MHz clock-tripled DX4 µP. The controller boasts a VAX MIPS rating of 68.34, 26.5% faster than controllers based on the i486DX2/66. The DX4, which operates from a 3.3V supply, uses less power than the i486DX2, reducing the controller's airflow requirements. One- and two-slot versions are available. Both sizes include hard disks (to 220 Mbytes in the 1-slot version, to 522 Mbytes in the 2-slot version), connectors for VGA or Super-VGA monitors, serial and parallel ports, and IEEE-488 interfaces. The 2-slot unit, which accepts an expansion kit that allows you to add two ISA bus boards, includes a 3.5-in. floppy-disk drive. Both units have connectors for external disk drives. From $7495. **National Instruments Corp**, Austin, TX. (512) 794-0100. **Circle No. 383**

Software uses PC's communication ports to analyze RS-232C traffic. DOS-based CommView V1.1 includes a windowed user interface. The software captures serial events, such as data characters, signal changes, and line errors, in real time. You can display the data in hexadecimal or text format in a set of windows, each of

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which contains a subset of the event information. You can also save the data to a log file in binary or text format. If you use the binary format, you can reload the data into the program. Around $160. **Microlynx Systems Ltd**, Calgary, AB, Canada. (403) 275-7346.
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Rubidium time-base counter ages at 50 parts/trillion/month. The 10-digit PM 6685R offers a relative measurement resolution of 250 parts/trillion. It warms up in six minutes to an error of 1 part/billion and in 30 minutes to 100 parts/trillion. Stability for one year is 500 parts/trillion, 100 times better than that of most oven-stabilized quartz oscillators, according to the vendor. The counter makes direct measurements to 300 MHz with a choice of preselectors to 1.3, 2.7, or 4.5 GHz. PIN diodes protect the RF inputs to withstand 12V rms. $10,645. **Fluke Corp**, Everett, WA. (800) 443-5853. **Circle No. 385**

One-piece test leads safely handle 1 kV and 15A. Model 4061 terminates at one end in a 4-mm shielded banana plug and at the other end in a 5¼-in. threaded stainless-steel probe that accepts accessories, such as a threaded clip, a plunger clip, and a spade lug. The 1m-long probes consist of flexible, finely stranded, silicone- or PVC-coated wire. Stock insulation colors are red and black; you can obtain other colors on special order. $8.68. **Mueller Electric Co**, Cleveland, OH. (216) 771-5225.
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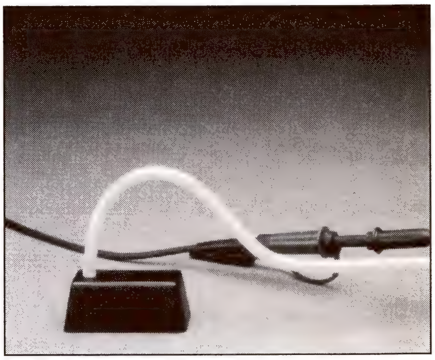

$49 SMD probe requires no special tooling. Quick Probe quickly connects to surface-mounted components without soldering. The unit maintains its position on the selected lead without drifting better than previous models could, according to the vendor. In addition, the base is heavier and has a non-skid pad. **R&R Design**, Longmont, CO. (303) 678-5004. **Circle No. 387**

Software links LabView to database packages. With DatabaseView for Windows, a $595 virtual-instrument (VI) library for National Instruments' graphics-based LabView for Windows data-acquisition software, you can create programs for information-intensive applications, such as automated test. DatabaseView permits using structured query language (SQL) to interact with databases directly from a LabView block diagram. **Ellipsis Inc**, Boston, MA. (800) 633-4866.
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5-MHz to 1-GHz signal-level meter maintains accuracy within ±1 dB from 0 to 50°C. The $2250 SignalScout signal-strength meter monitors three channels plus a reference (pilot) level simultaneously or separately and produces spectrum displays with 30- to 300-kHz resolution bandwidth. A software package (normally $500) that

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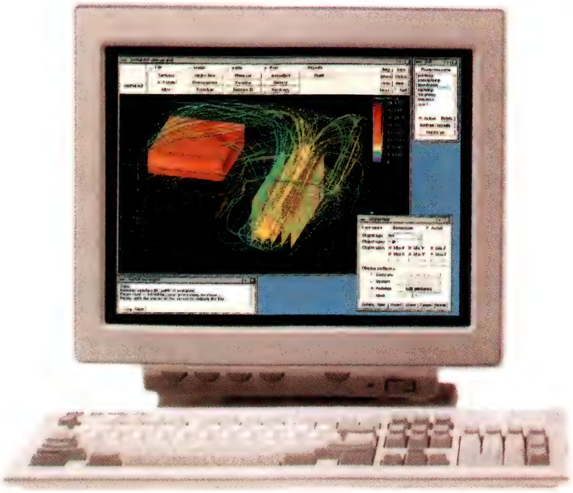

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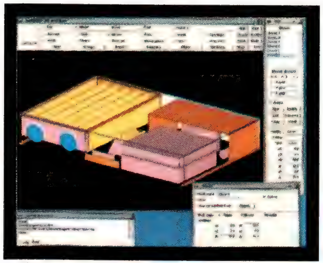

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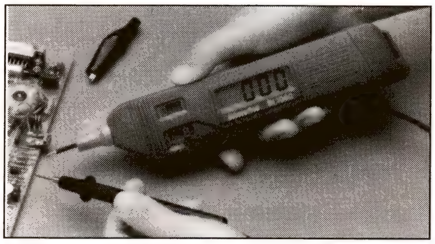
lets you define test sequences, download them to the meter, and upload test results to a PC or printer, is free with purchases of the meter until December 1. **Tektronix Inc**, Beaverton, OR. (800) 835-9433. **Circle No. 389**

\$399 5.5×4.2-in. data-acquisition board acquires 16 channels at 110k samples/sec. The CIO-DAS16/Jr offers 12-bit resolution. You can set the input range to five bipolar and five unipolar values, the most sensitive of which is 0.625V. The vendor claims compatibility with software and accessories for use with competitive DAS-16 boards. **Computer Boards Inc**, Mansfield, MA. (508) 261-1123. **Circle No. 390**

\$49.95 $3\frac{1}{2}$-digit pocket DMM selects ac or dc measurements. The $4\frac{3}{4}\times2\frac{5}{8}\times1$-in. WP2600, which receives power from two AAA cells, has five dc and four ac voltage ranges and measures dc and ac current to 10A. It also tests diodes and provides an audible continuity indication. The meter, whose inputs are protected against overvoltage on all ranges, detects whether the input signal is ac or dc and selects the appropriate mode. **Windward Products**, Santa Clara, CA. (408) 987-7734. **Circle No. 391**

SBus data-acquisition board takes 5M 12-bit samples/sec on two channels. The ADDA1205DX includes 16 Mbytes of dual-ported RAM, four TTL inputs, four TTL outputs, and two 12-bit DACs. It can simultaneously service all of these without compromising the ADC sample rate. The sample rate is programmable down to 51.15 μsec/sample. A pipeline mode allows you to use the RAM for outputting DAC and TTL signals while inputting ADC and TTL signals. \$4995; without DACs, \$4295; with a single ADC, \$3395. **Ultraview Corp**, Fremont, CA. (510) 657-9501. **Circle No. 392**

ASIC expands coverage of Asset scan-test diagnostic system. Incorporating the ParaScan ASIC in a multichip module or pc board makes it possible to perform non-IEEE-1149.1 logic testing, improves access to the unit under test during embedded testing, and increases the coverage of tests conducted via the edge connector. The \$225 ASIC, which is packaged in a 144-pin QFP, includes 66 bidirectional inputs and outputs, each with its own control cell. **Intellitech Corp**, Meredith, NH. (603) 279-6308. **Circle No. 393**



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Lab supplies deliver prodigious currents. The EA-9000 series of laboratory power supplies come in three voltage/current combinations: 0 to 18V at 300A, 0 to 36V at 180A, and 0 to 72V at 90A. The power-factor-corrected units require 3-phase input power. The supplies feature automatic remote sensing, 0.15% stability, programmability, and analog or LCD meters. Rack mounting and an IEEE 488 interface are optional. $3000 (2 kW), $8000 (6 kW), delivery from stock. **Electro Automation Co**, Lawrence, MA. (508) 687-6411. **Circle No. 374**

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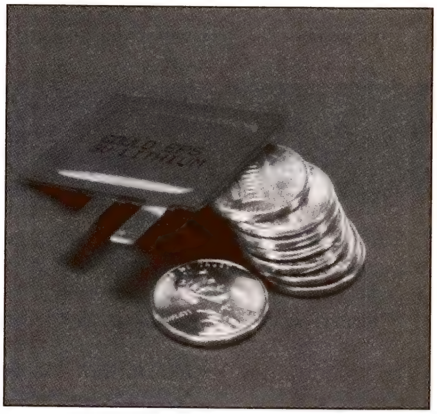

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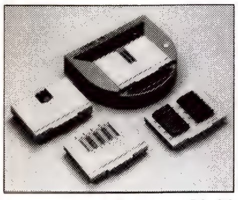

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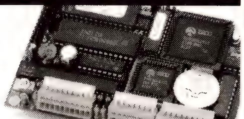

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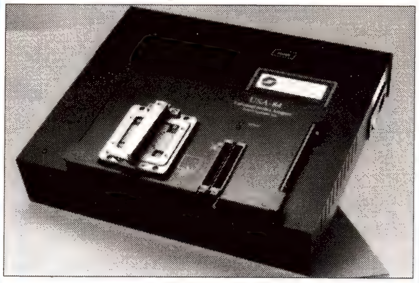

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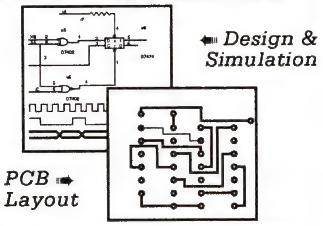

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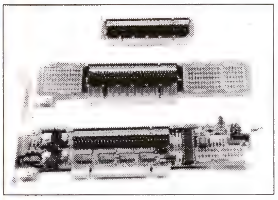

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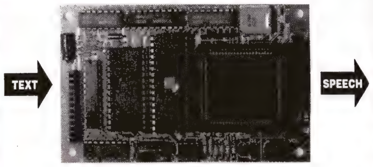

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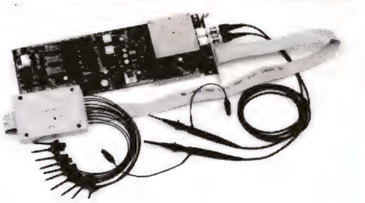

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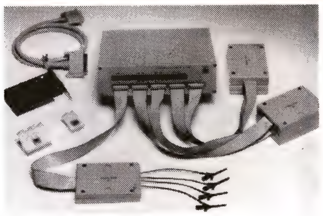

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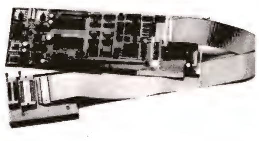

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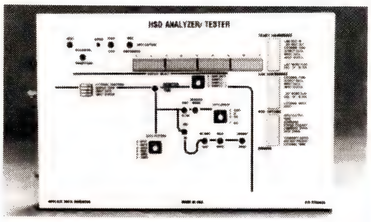

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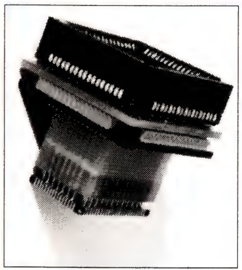

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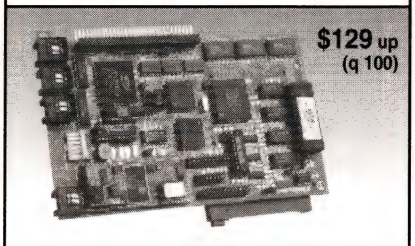

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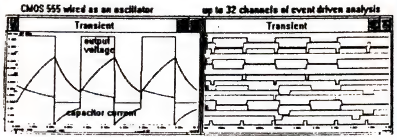
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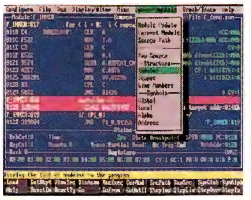

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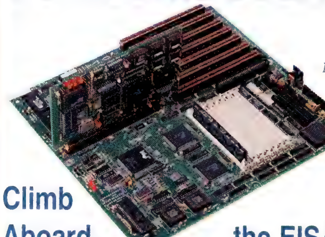

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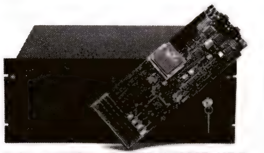

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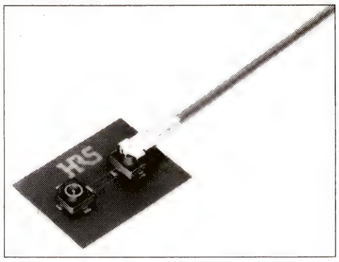

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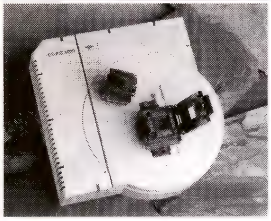

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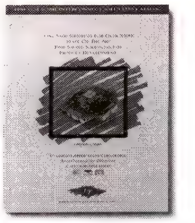

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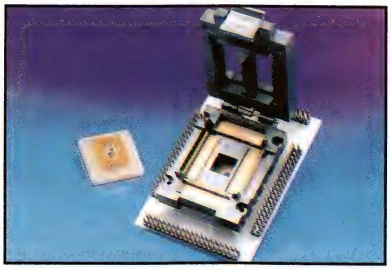

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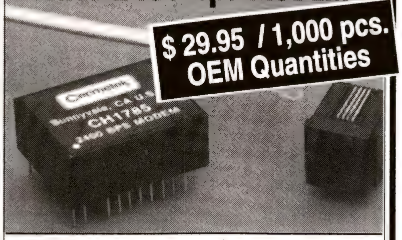

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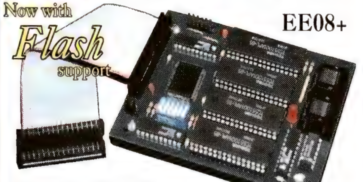

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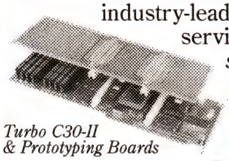

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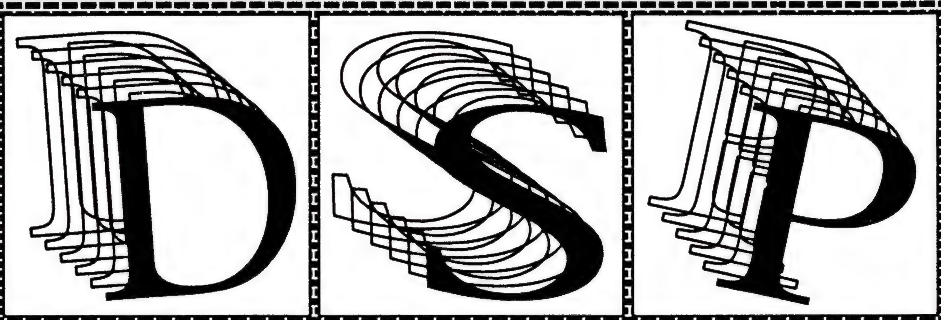

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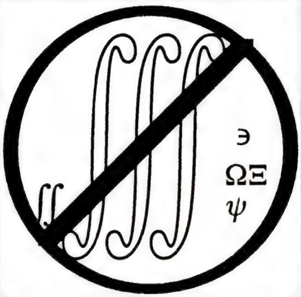

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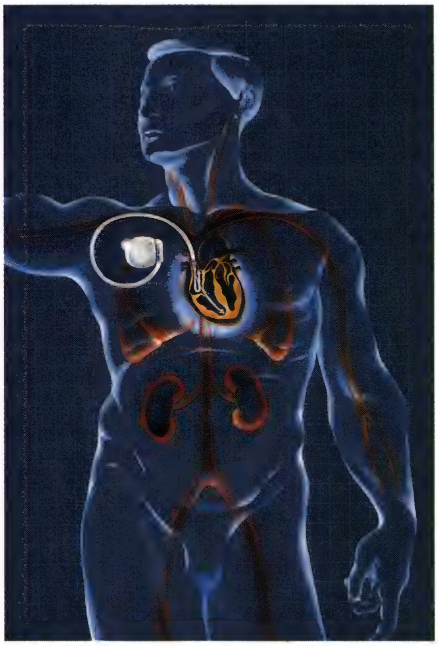

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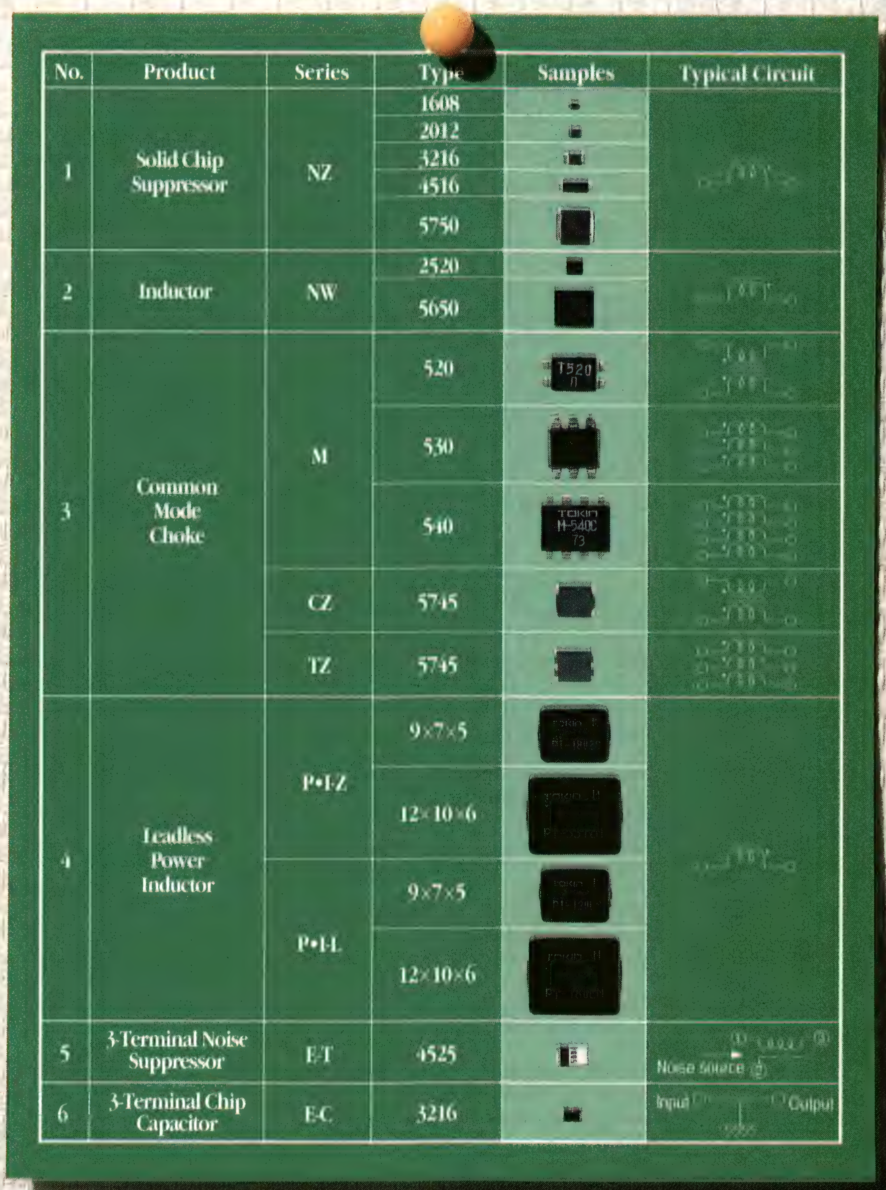

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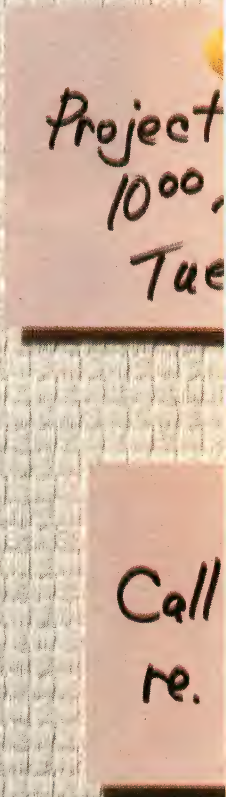

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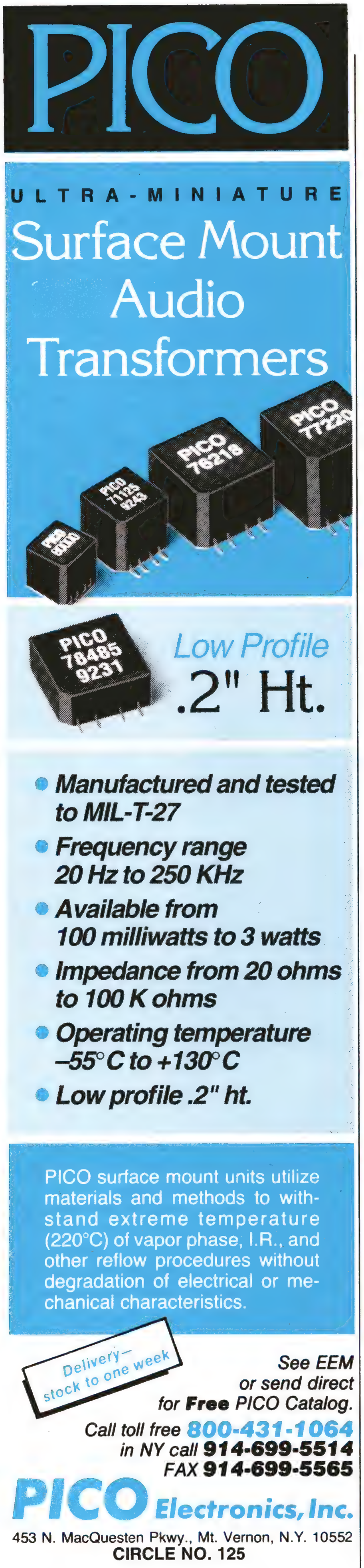

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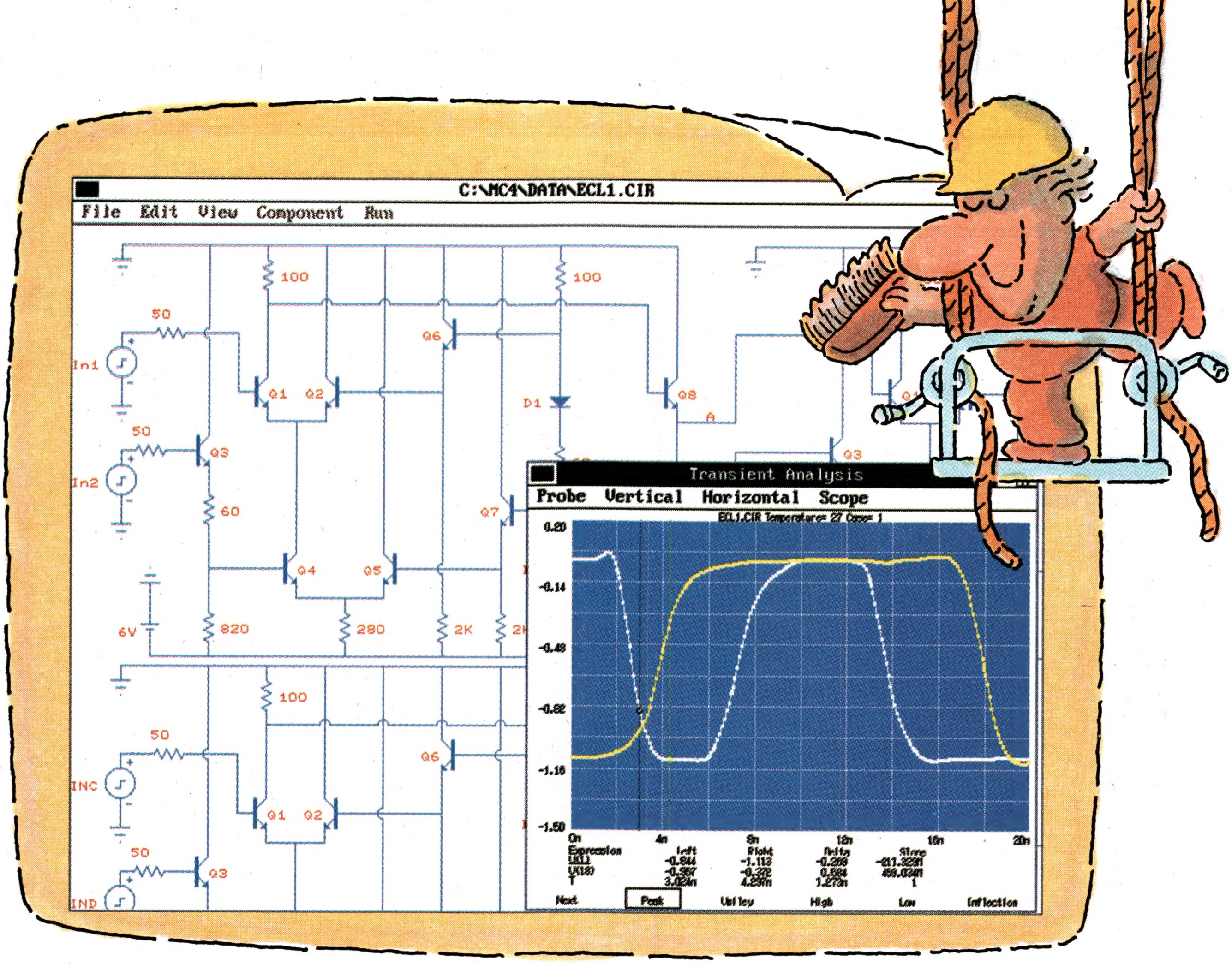

Expression	Left	Right	Delta	Slope
V(1)	-0.844	-1.113	-0.269	-211.329M
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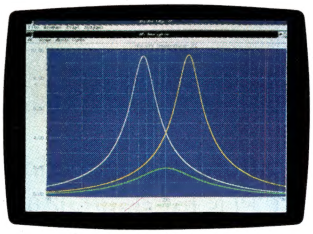

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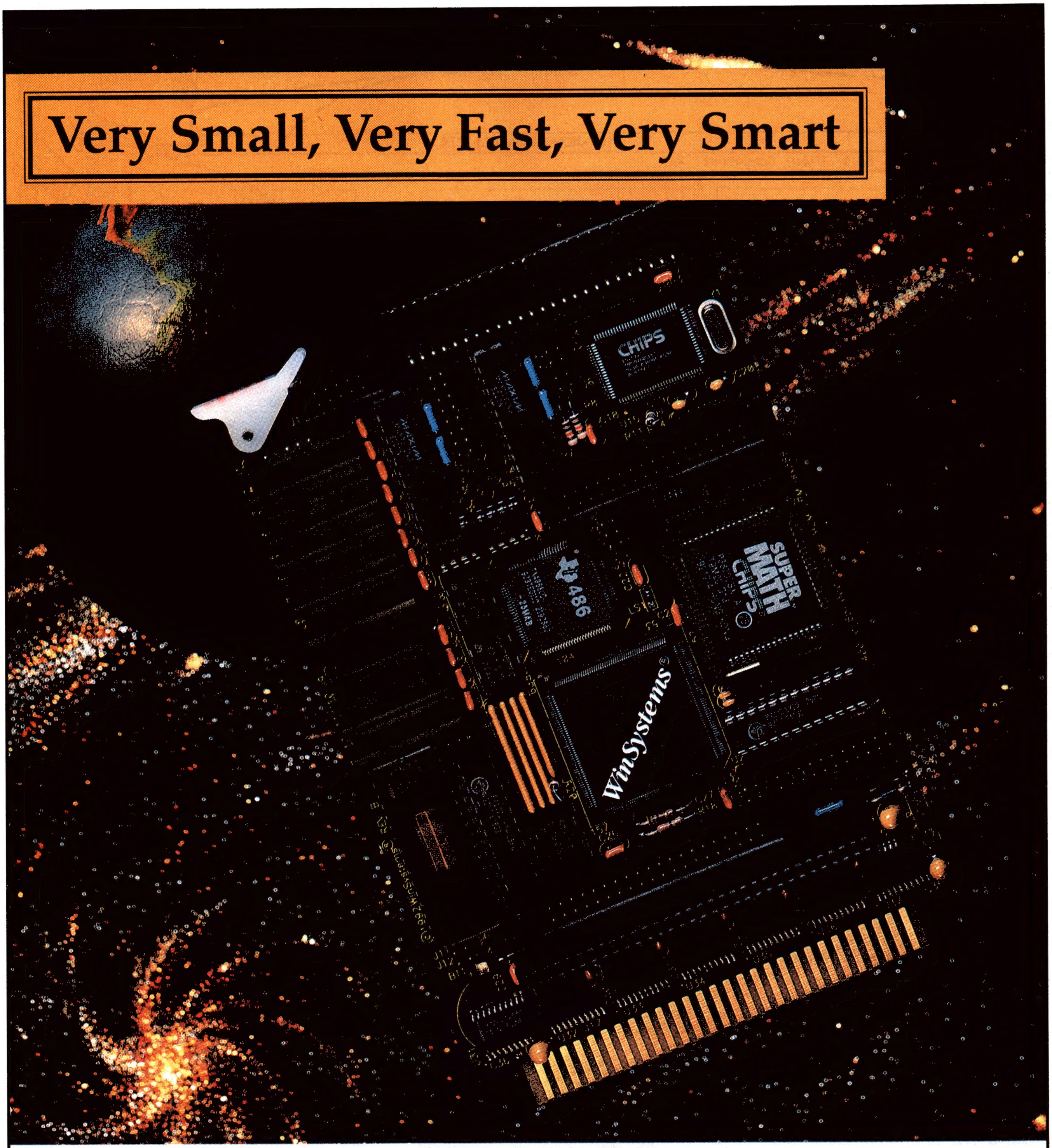

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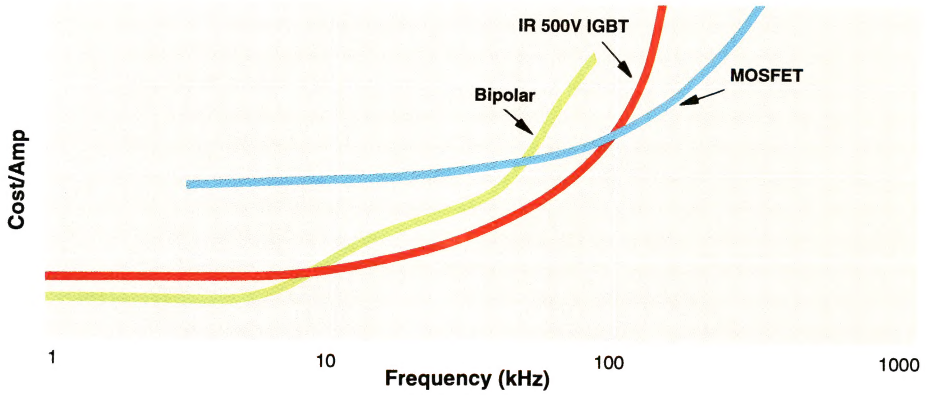

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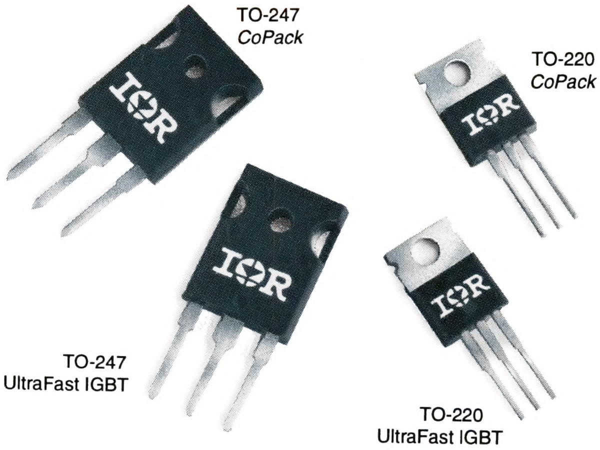

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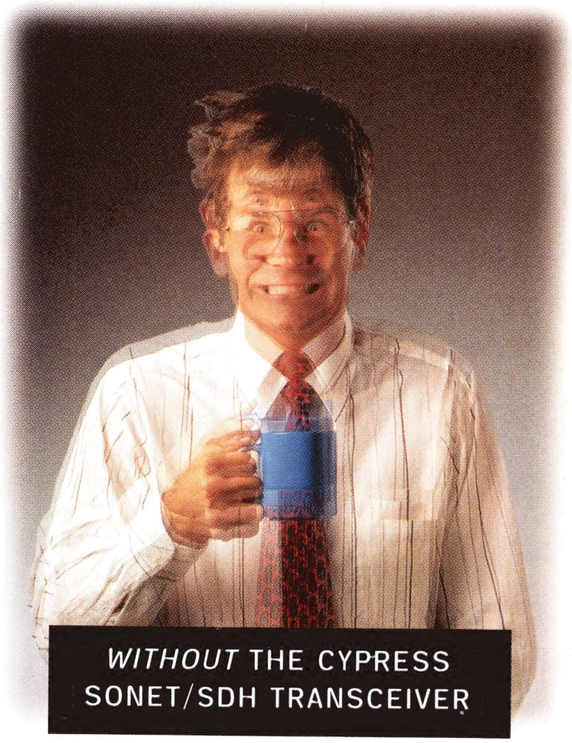
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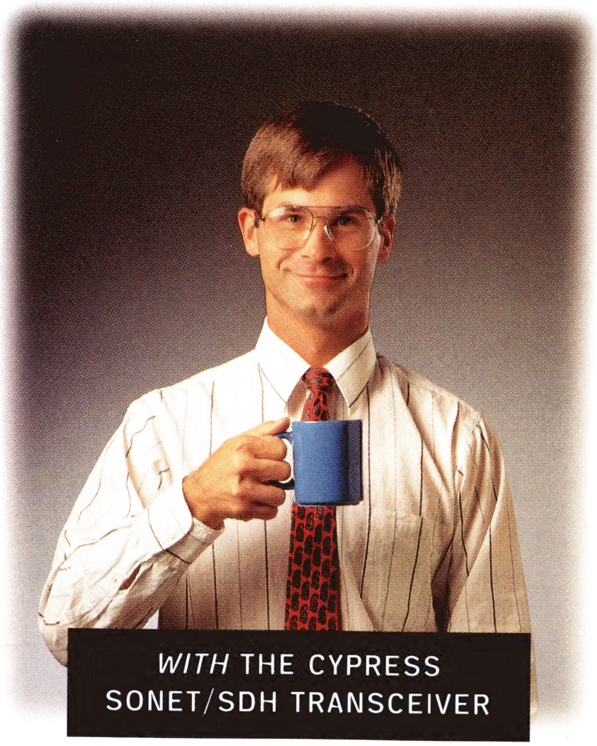
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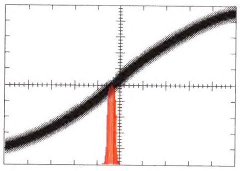
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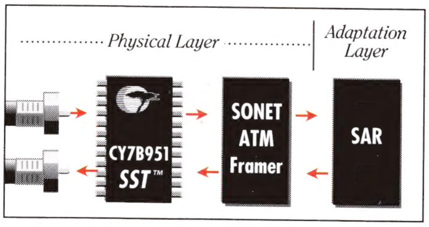

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